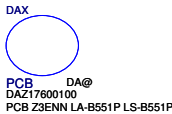


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Model Name : Z3ENN
File Name : LA-B551PR10
BOM P/N : 4319TUBOL01~10



Compal Confidential

NIKE MB LA-B551P

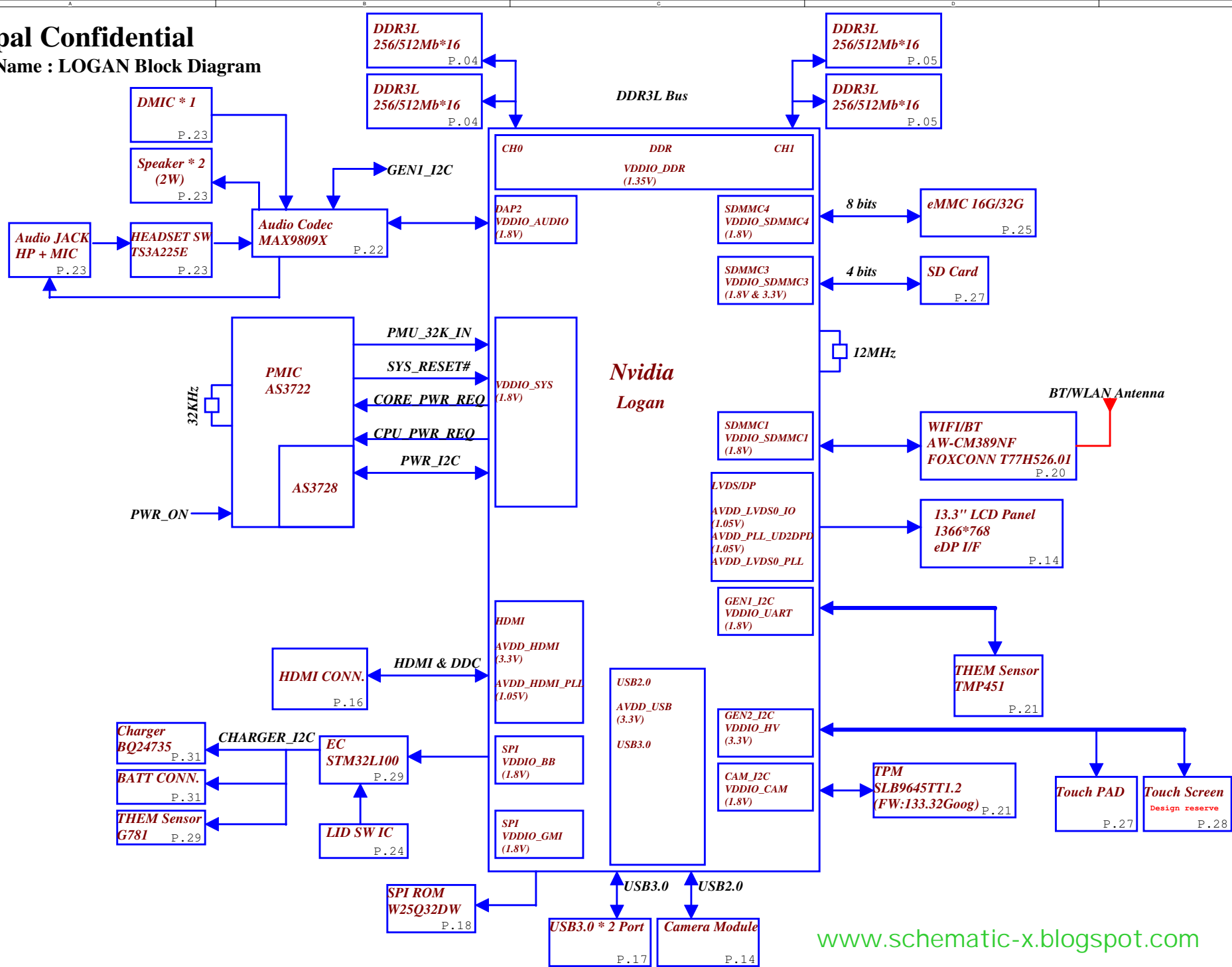
Nvidia LOGAN Processor

2014-05-28

REV: 1.0

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Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title Cover Page	
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Compal Confidential
Model Name : LOGAN Block Diagram



www.schematic-x.blogspot.com

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Voltage Rails

Power Plane	Description	ACTIVE	SUSPEND	DEEP SLEEP	OFF
VIN	Adapter power supply (12V)				
BATT+	Battery power supply				
B+	AC or battery power rail for power circuit.				
VDD_5V0_SYS	For All Device standby mode				
VDD_3V3_SYS	For All Device standby mode				
VDD_1V8_PMU	For All Device standby mode				
V_RTC_1V8	PMU RTC power rail				
+VDD_1V35_MEM	DDR3L power rail & TEGRA DDR power rail				
VDD_0V675_DDR3_VREF	For DDR VREFDQ & VREF CA				
VDD_1V2_CORE_AP	For TEGRA core logic				
VDD_1V0_CPU	For TEGRA CPU VDD				
VDD_1V05_PLL_AP	AVDD_PLL_P_C, AVDD_PLL_X, AVDD_PLL_M, AVDD_PLL_U, AVDD_PLL_E				
VDD_1V8_PMU	For TEGRA AVDD_OSC, VDDIO_SYS				
VDD_1V05_PLL_AP	For TEGRA VDDIO_DDR_HS				
VDD_1V8_PMU	For TEGRA VDDIO_GMI,				
VDD_1V05_PLL_AP	For TEGRA AVDDIO_USB3, AVDD_USB3_PLL				
V_USB_3V3	For TEGRA AVDD_USB, HVDD_USB3				
VDD_1V8_PMU	For TEGRA VDDIO_CAM, VDDIO_SDMMC4, AVDD_USB_PLL				
VDD_3V3_HV_AP	For TEGRA VDDIO_HV				
VDD_1V05_PLL_AP	For TEGRA AVDD_HDMI_PLL				
AVDD_3V3_HDMI_TEGRA_S	For TEGRA AVDD_HDMI				
VDD_1V05_PLL_AP	For TEGRA AVDD_DSI_CSI_PLL				
V_MIPI_1V2	For TEGRA AVDD_DSI_CSI				
VDD_3V3_SD_CARD	For SD card Power				
V_MICROSD_IO	For TEGRA VDDIO_SDMMC3				
VDD_1V8_PMU	For TEGRA VDDIO_BB				
VDD_1V8_PMU	For TEGRA VDDIO_Audio,VDDIO_SDMMC1, VDDIO_UART				
VDD_1V8_PMU	For eMMC VCCQ Power rail				
VDD_2V85_EMMC	For eMMC VCC Power rail				
VDD_2V85_EMMC	For eMMC Power rail				
VDD_5V0_SYS	For CODEC AMP Power				
+MICBIAS	For MIC signal				
VDD_1V8_PMU	For CODEC Power				
V_MIPI_1V2	For eDP bridge Power				
VDDC_1V8_EDP	For eDP bridge Power				
VDD_3V3_SYS	For Cap sensor Power rail				
BL_12V	For LCD backlight Power rail				
VDD_3V3_LCM	For LCD Power rail				
VDD_3V3_LCM	For Touch Control Power rail				
VDD_3V3_SYS	For 2M Front Camera & ALS Power rail				
V_SENSOR_2V85	For GYRO & COMPASS rail				
VDD_3V3_SYS	For Wireless KB Power rail				
V_CAM_2V8	For 8M Rear CAMERA AVDD				
VDD_1V8_PMU	For 8M Rear CAMERA VDDIO				
V_VCM_2V8	For 8M Rear CAMERA VCM_VDD				
VDD_3V3_SYS	For WIFI VBAT Power rail				
VDD_1V8_PMU	For WIFI VIO Power rail				
VDD_3V3_SYS	For NFC VBAT Power rail				
VDD_1V8_PMU	For NFC PVDD Power rail				
VDD_3V3_SYS	For GPS VDD Power rail				
VDD_1V8_PMU	For GPS VDDIO Power rail				
+GPS_AUX_OUT	For GPS LNA Power				
VDD_3V3_SBY_EC(EC_AVCC)	For MCU Power				

BOM Config

Non-Touch

4319TUBOL01 (SMT MB AB551 Z3ENN HYN 2G KIN 16G HDMI)
EMI@/DA@/HYN2G@/HYN16G@/AZURE@

4319TUBOL02 (SMT MB AB551 Z3ENN T50 2G/16G HDMI)
EMI@/DA@/HYN2G@/HYN16G@/AZURE@

4319TUBOL03 (SMT MB AB551 Z3ENN T50 4G/32G HDMI)
EMI@/DA@/HYN4G@/HYN32G@/AZURE@

4319TUBOL04 (SMT MB AB551 Z3ENN T50 2G/32G HDMI)
EMI@/DA@/HYN2G@/HYN32G@/AZURE@

4319TUBOL05 (SMT MB AB551 Z3ENN T50 4G/16G HDMI)
EMI@/DA@/HYN4G@/HYN16G@/AZURE@

4319TUBOL06 (SMT MB AB551 Z3ENN HYN 2G KIN 16G P2 HDMI)
EMI@/DA@/HYN2G@/KIN16G@/AZURE@

Touch

4319TUBOL07 (SMT MB AB551 Z3ENN T50 2G/16G T HDMI)
TS@/EMI@/DA@/HYN2G@/KIN16GA@/AZURE@

4319TUBOL08 (SMT MB AB551 Z3ENN T50 4G/32G T HDMI)
TS@/EMI@/DA@/HYN4G@/HYN32G@/FOXCO@

4319TUBOL09 (SMT MB AB551 Z3ENN T50 2G/32G T HDMI)
TS@/EMI@/DA@/HYN2G@/HYN32G@/FOXCO@

4319TUBOL10 (SMT MB AB551 Z3ENN T50 4G/16G T HDMI)
TS@/EMI@/DA@/HYN4G@/KIN16G@/FOXCO@

BTO Option Table

BTO Item	BOM Structure
EMI Part	EMI@
EMI Reserve Part	@EMI@
ESD Reserve Part	@ESD@
PCB	DA@
Connector	CONN@
UN-MOUNT	@
eMMC	KIN16G@
	HYN16G@
	KIN32G@
	HYN32G@
	KIN16GA@
DDR3L	HYN2G@
	HYN4G@
	KIN2G@
WIFI/BT	AZURE@
	FOXCO@
Touch Screen	TS@

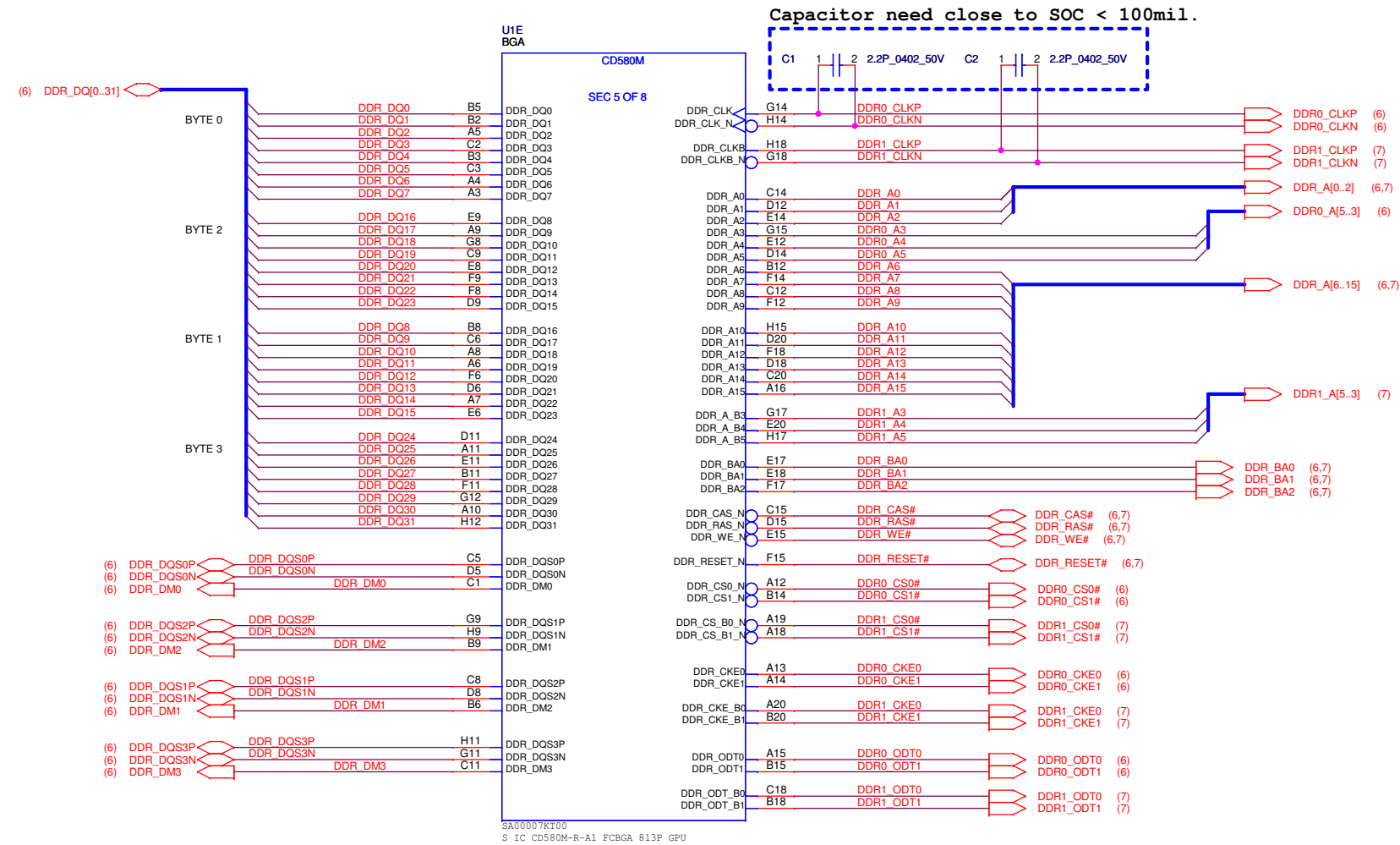
Bus	Device	Address	Write	Read
PWR_I2C	PMU	40	80	81
CHARGER_I2C	Battery	0B	16	17
GEN1_I2C	Thermal	4C	98	99
	Audio	10	20	21
GEN2_I2C	T/P	15	CE	CF
	T/S	78	94	95
HDMI_DDC	HDMI			
TPM_I2C	TPM	20	40	41

NIKE (Z3ENN) strapping						
Board ID		SMT Data	HW GPIOs [BD_ID_STRAP[3:0]]	SW Hex	PCB version	HW_ID(SA)
	Proto		0000	0X00		
Non Touch SKU	EVT		0001	0X01	PR01	
Non Touch SKU	DVT	2014/4/1	000Z	0X02	PR02	
Non Touch SKU	PVT	2014/5/7	0010	0X03	PR03/PP04/PR05	
Non Touch SKU	Pre-MP / MP	2014/7/4	0011	0X04	PR10	
Touch SKU	DVT	2014/6/21	001Z (suggestion)	0X05	PR06	
Touch SKU	PVT	2014/8/5	00Z0 (suggestion)	0X06	PR10	
Touch SKU	Pre-MP / MP	2014/8/27	00Z1 (suggestion)	0X07	PR10	

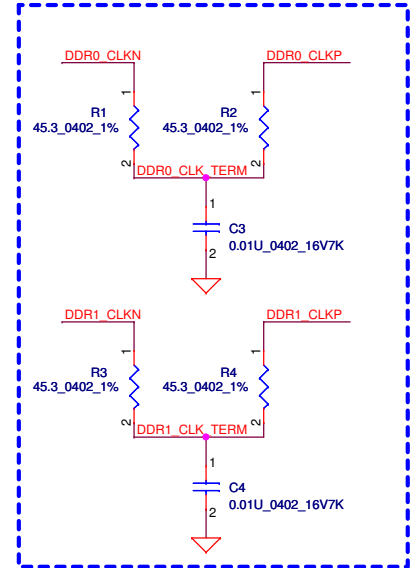
MEM ID		GPIOs (RAMCODE[3:0])
0	2GB Micron	0000
1	2GB Hynix	0001
2	2GB Elpida	0010
3	4GB Micron	0011
4	4GB Hynix	0100
5	4GB Elpida	0101
6	2GB Kingston	0110

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CD580M: CH0 MEMORY I/F

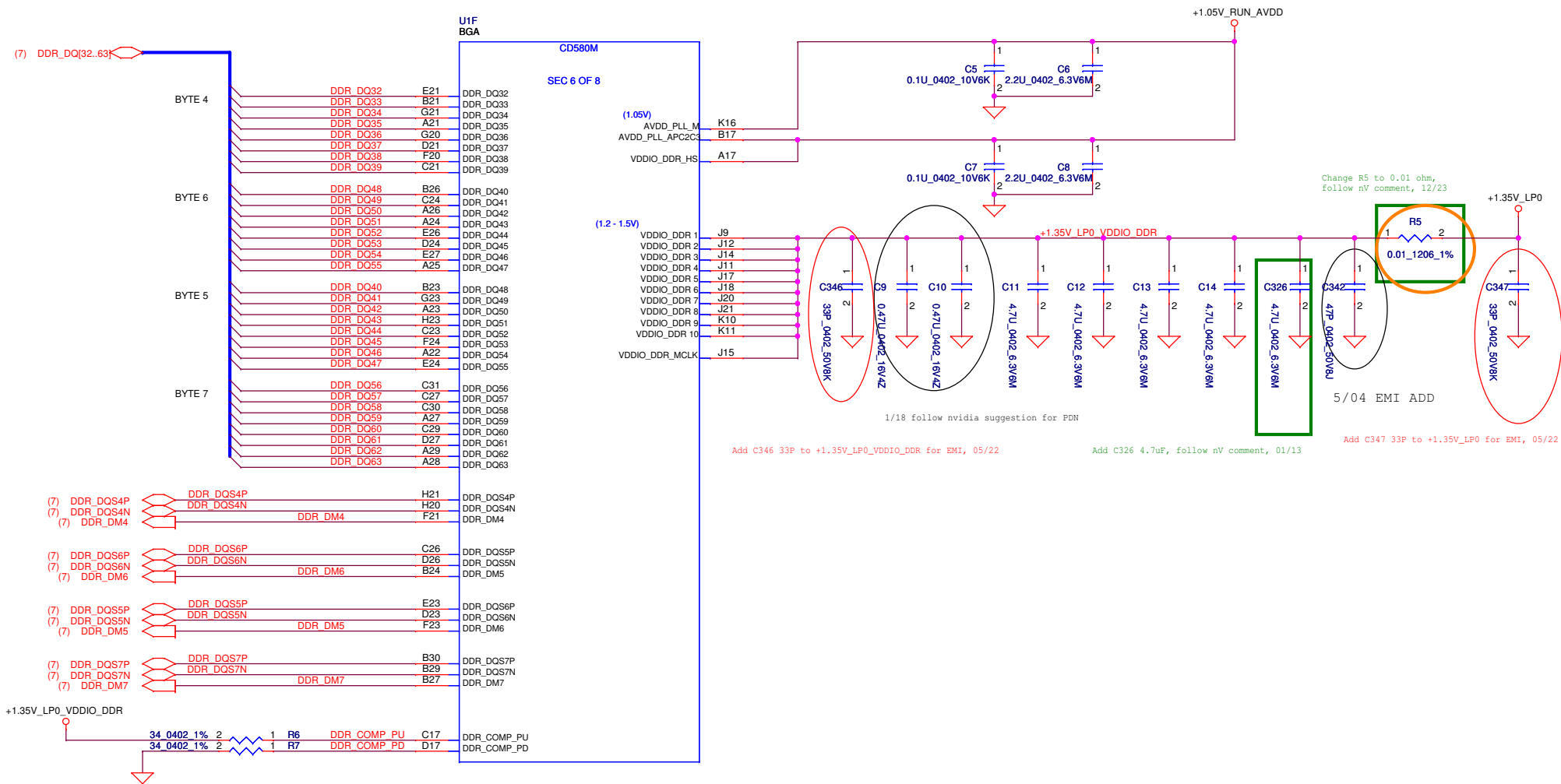


Note:Place at the T-point



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								DDR3L (Channel 0)			
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								Z3ENN M/B LA-B551P		0.1	
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CD580M: CH1 MEMORY I/F



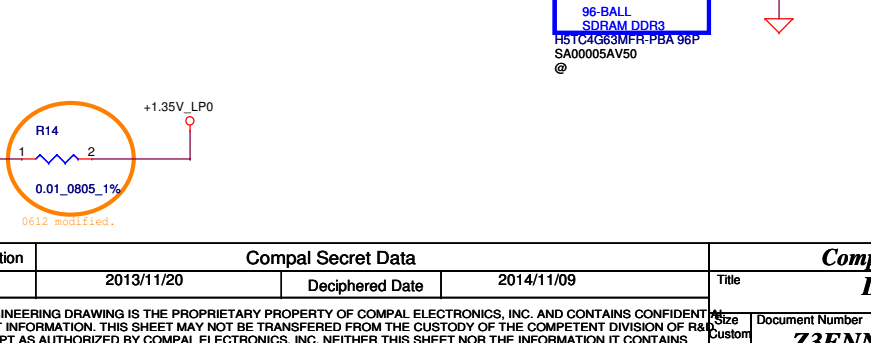
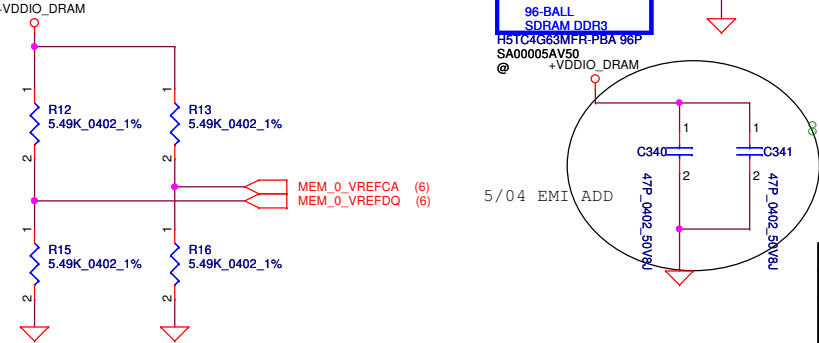
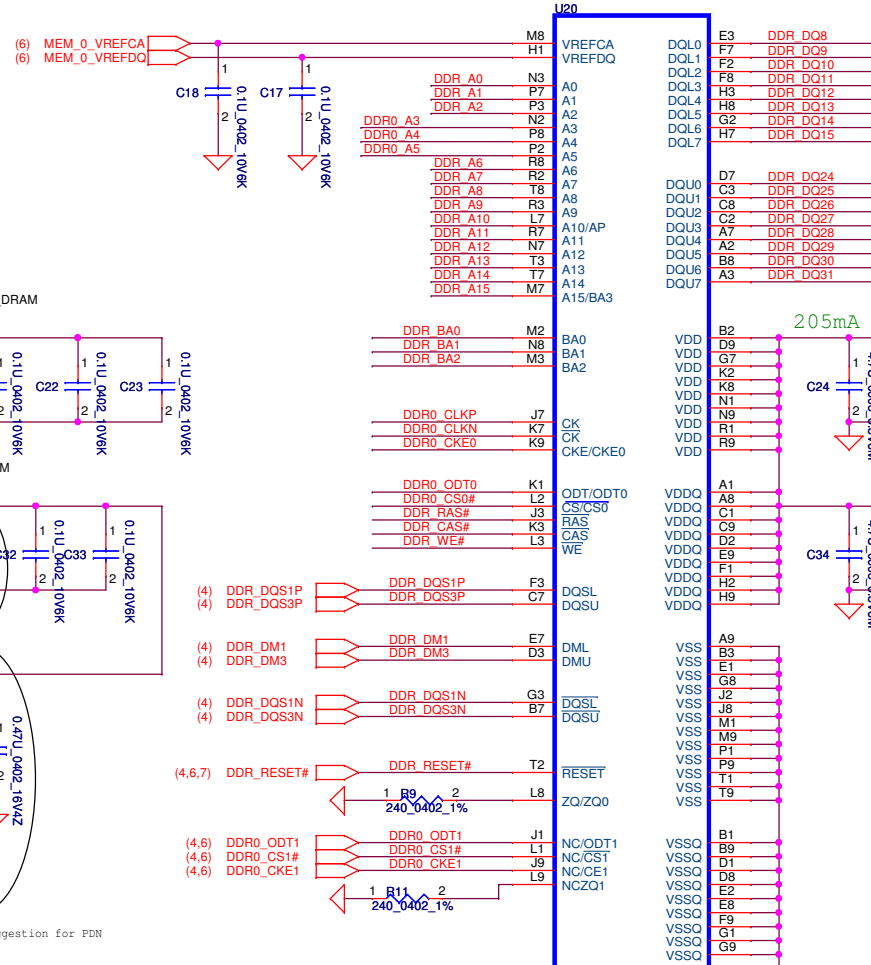
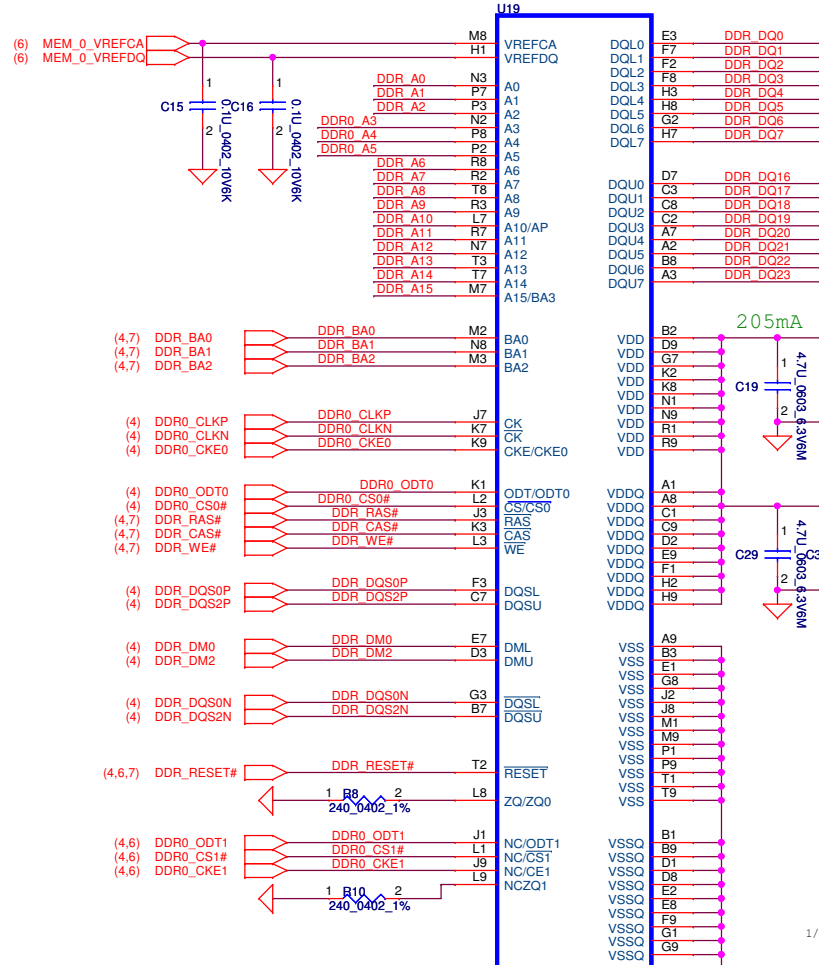
256Mx16 DDR3 *4==>2048MB
512Mx16 DDR3 *4==>4096MB

(4) DDR_DQ[0..31]
(4,7) DDR_A[0..2]
(4) DDR0_A[5..3]
(4,7) DDR_A[6..15]

U19 HYN2G@
SA00005AV50
S IC D3 256M16/1600 H5TC4G63AFR-PBA ABO!
U19 HYN4G@
SA00006WZ40
S IC D3 512M16/1600 H5TC8G63AMR-PBA ABO!

U20 HYN2G@
SA00005AV50
S IC D3 256M16/1600 H5TC4G63AFR-PBA ABO!
U20 HYN4G@
SA00006WZ40
S IC D3 512M16/1600 H5TC8G63AMR-PBA ABO!

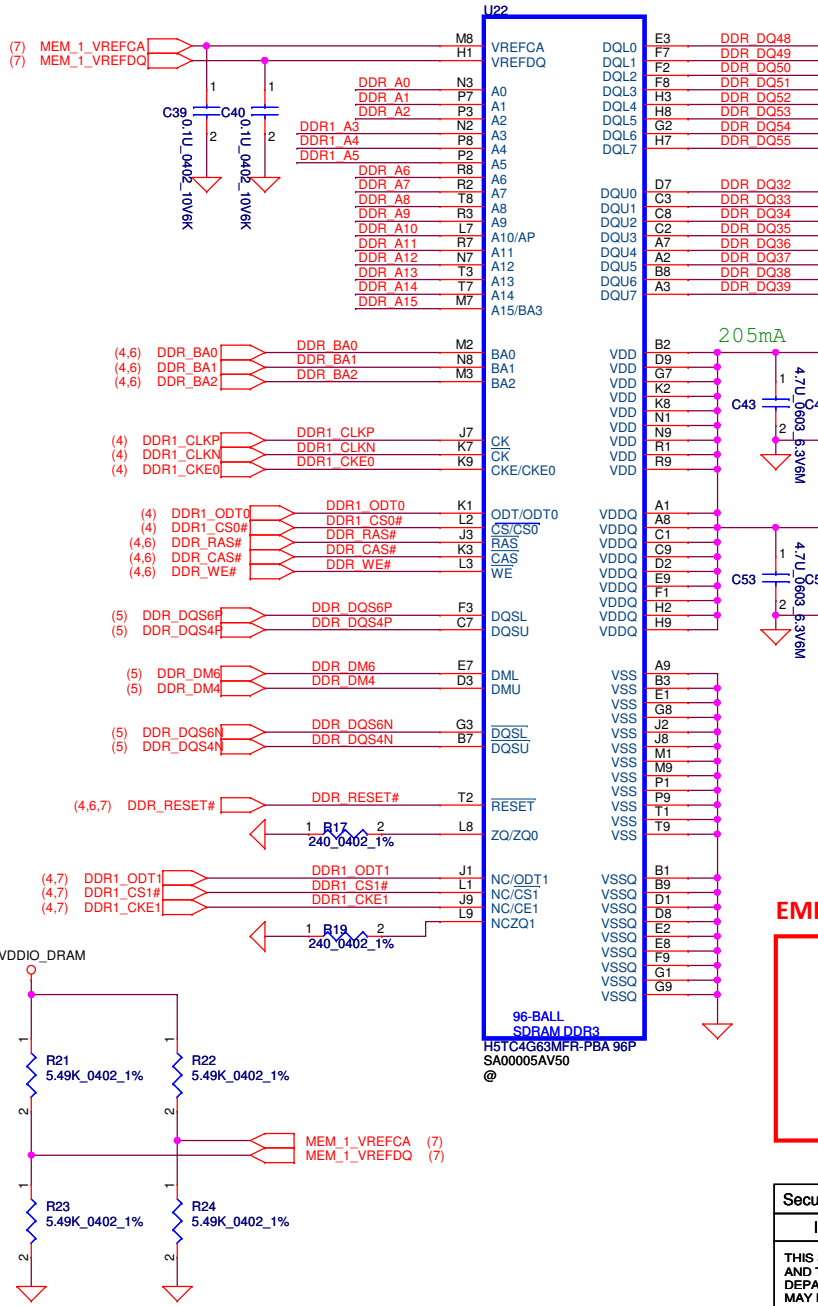
U19 KIN2G@
SA00007X410
S IC D3 256M16/1600 D2516EC4BXGGB ABO!
U20 KIN2G@
SA00007X410
S IC D3 256M16/1600 D2516EC4BXGGB ABO!



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					DDR3L CH0
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256Mx16 DDR3 *4==>2048MB
512Mx16 DDR3 *4==>4096MB

- (5) DDR_DQ[32..63]
(4,6) DDR_A[0..2]
(4) DDR1_A[5..3]
(4,6) DDR_A[6..15]



U22 HYN2G@
SA00005AV50
S IC D3 256M16/1600 H5TC4G63AFR-PBA ABO!

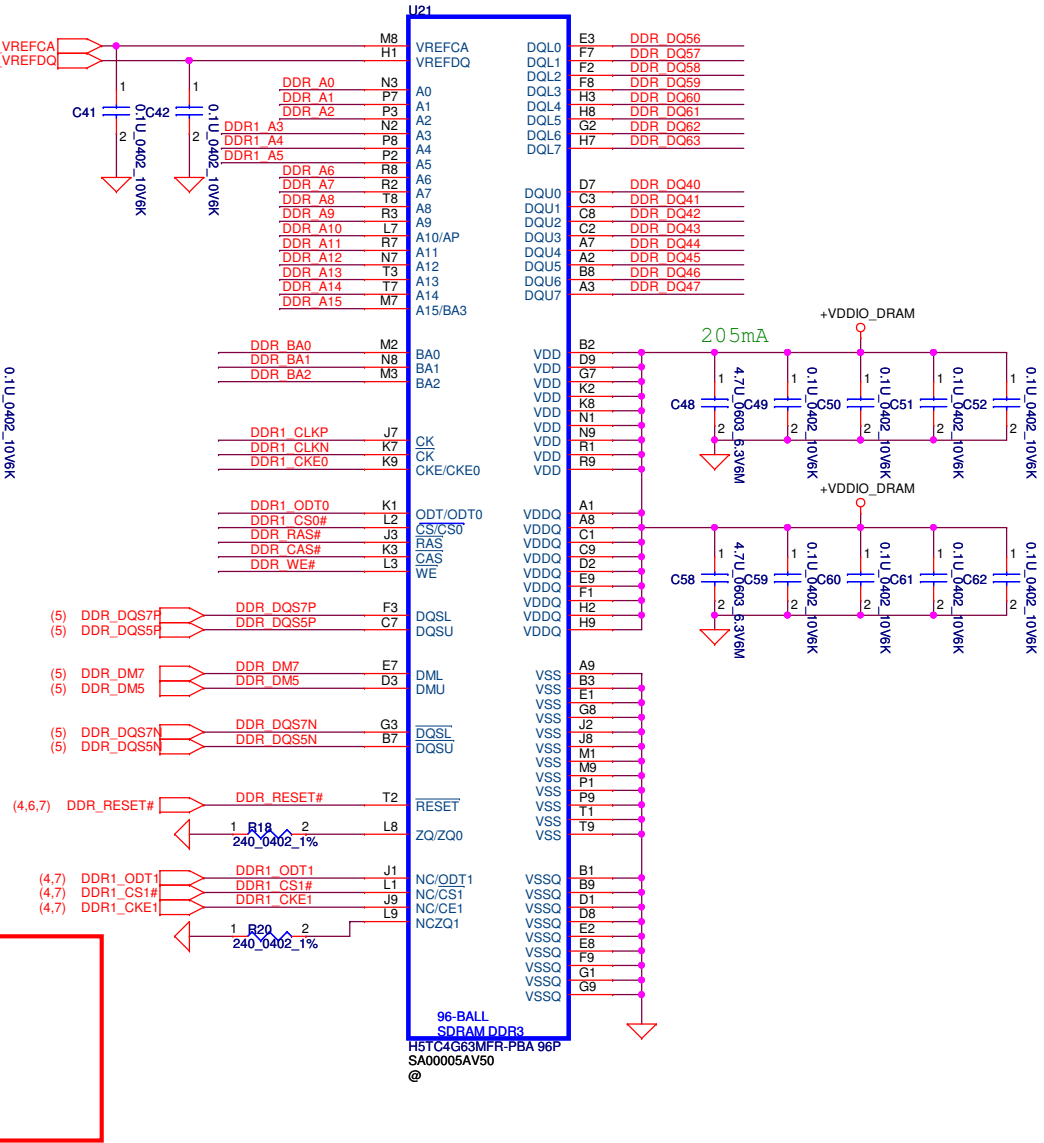
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SA00006WZ40
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U21 HYN2G@
SA00005AV50
S IC D3 256M16/1600 H5TC4G63AFR-PBA ABO!

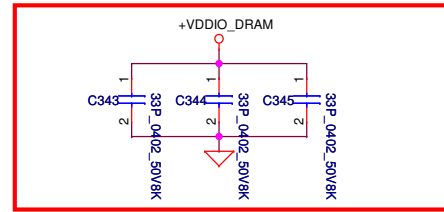
U21 HYN4G@
SA00006WZ40
S IC D3 512M16/1600 H5TC8G63AMR-PBA ABO!

U22 KIN2G@
SA00007X410
S IC D3 256M16/1600 D2516EC4BXGGB ABO!

U21 KIN2G@
SA00007X410
S IC D3 256M16/1600 D2516EC4BXGGB ABO!



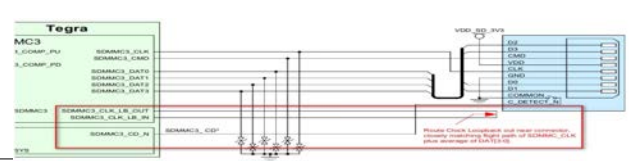
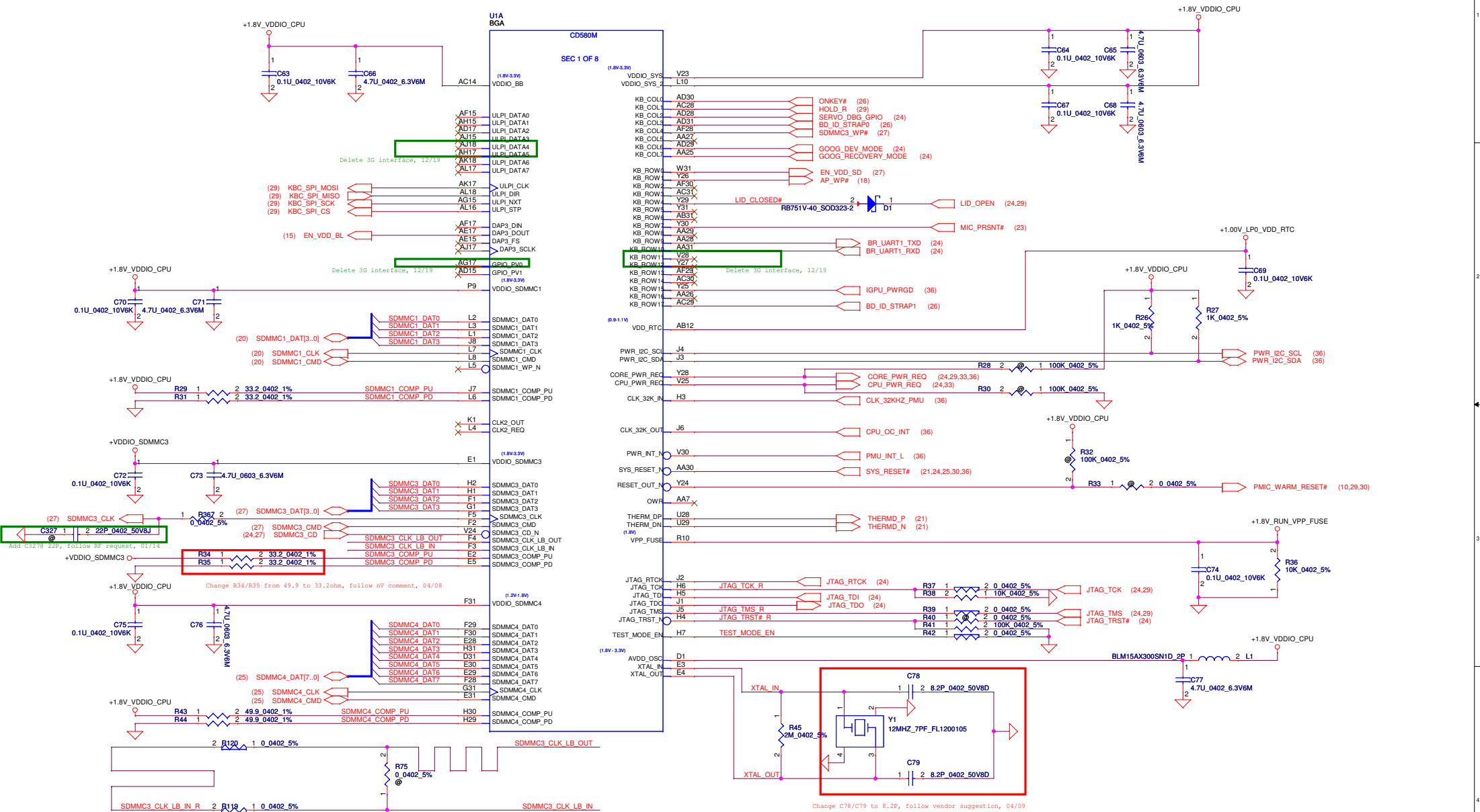
EMI, close to C50/C57/C28



Add C343/C344/C345 33P to +VDDIO_DRAM for EMI, 05/22

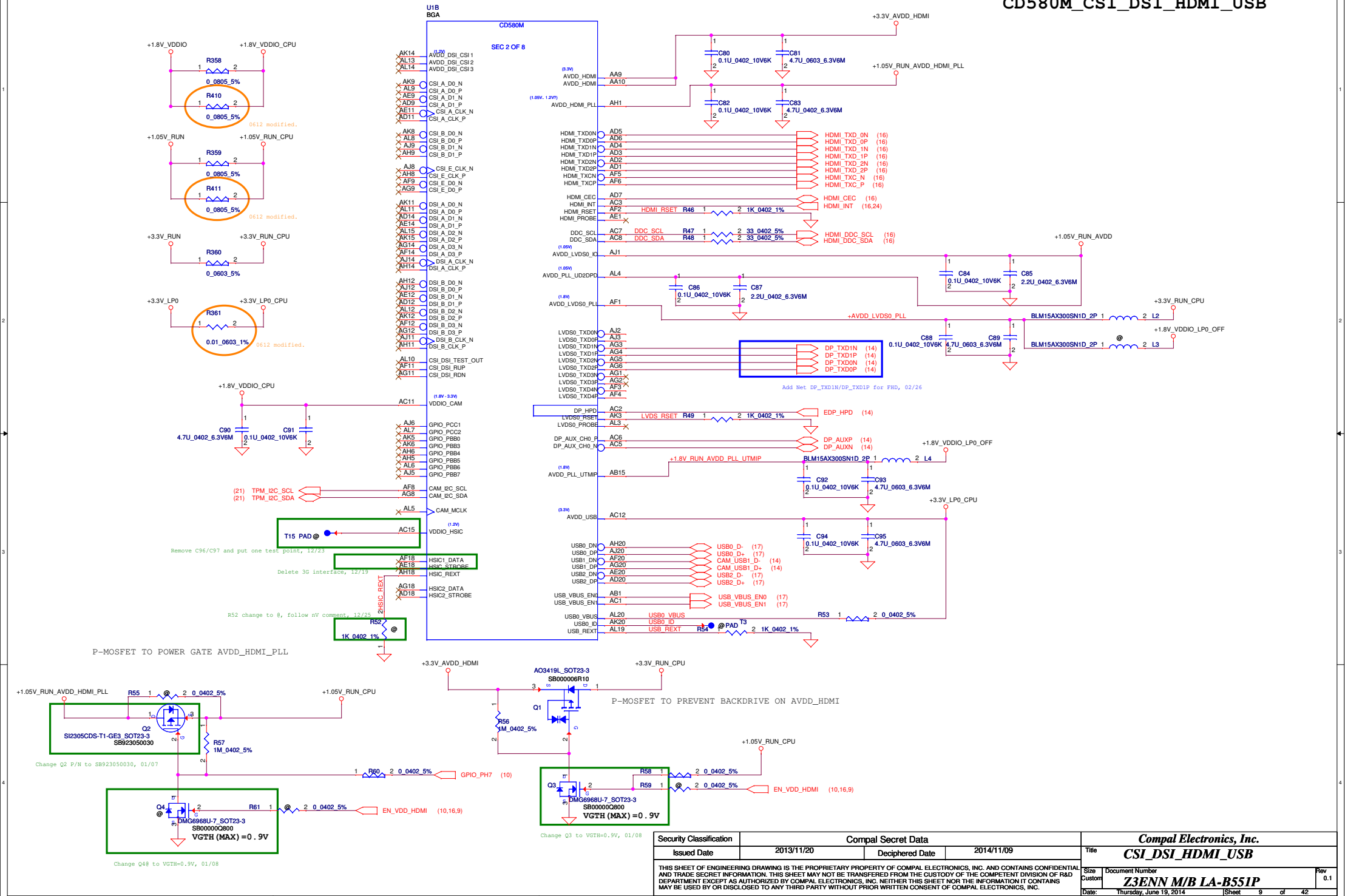
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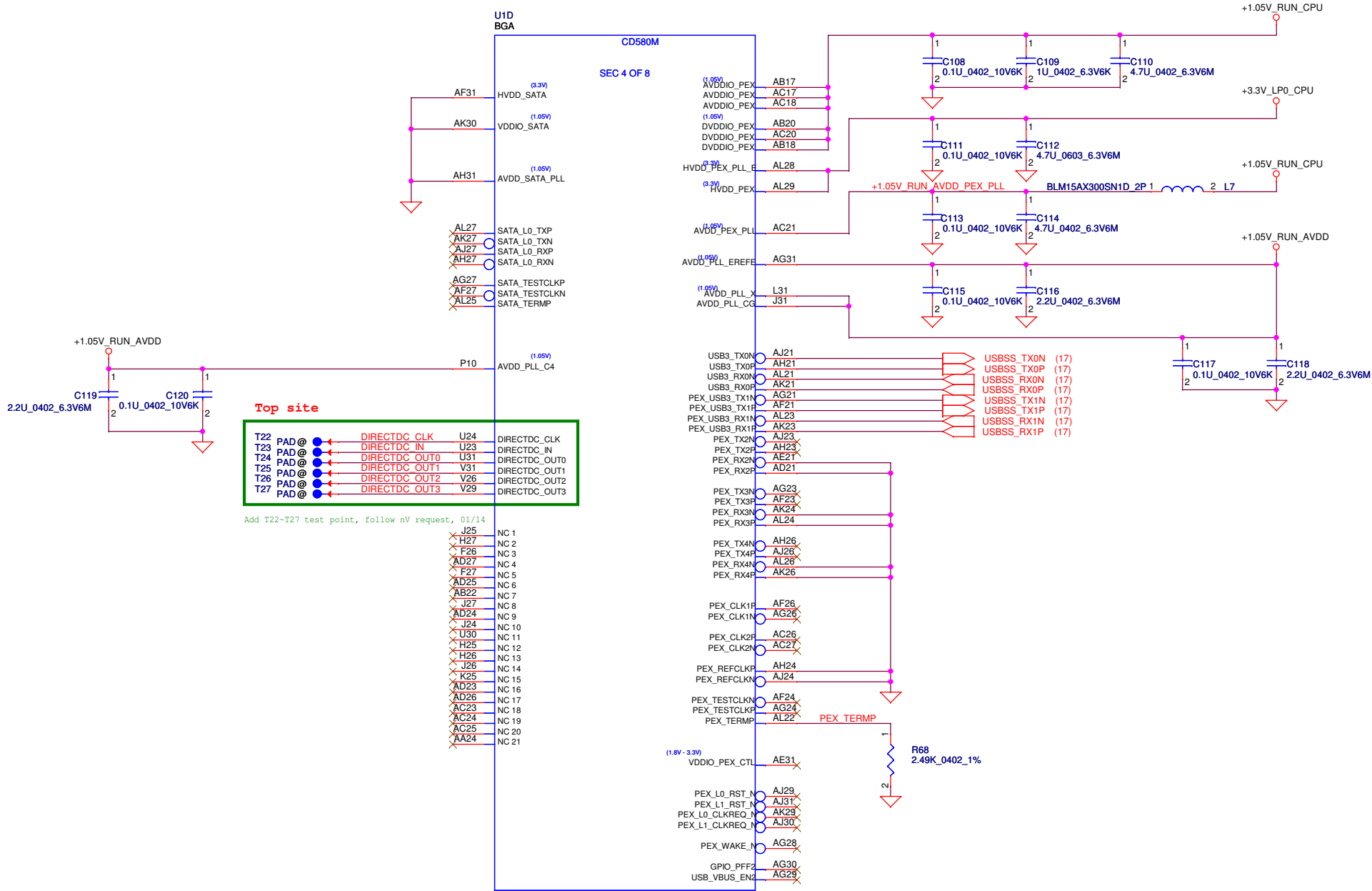
CD580M_SDMMC_ULPI_JTAG



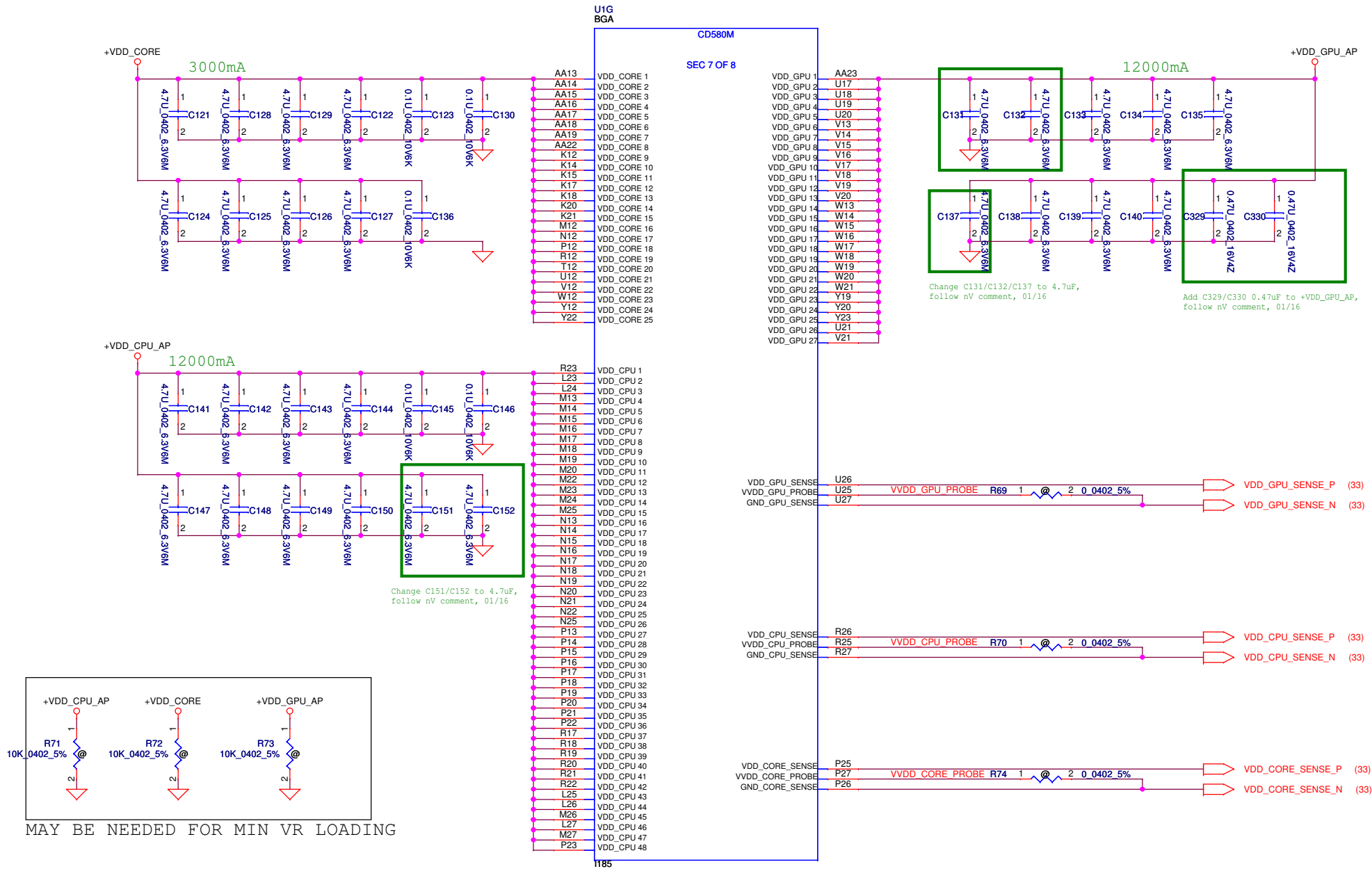
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		SDMMC_ULPI_JTAG			
Size	Document Number				Rev
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CD580M_CSI_DSI_HDMI_USB

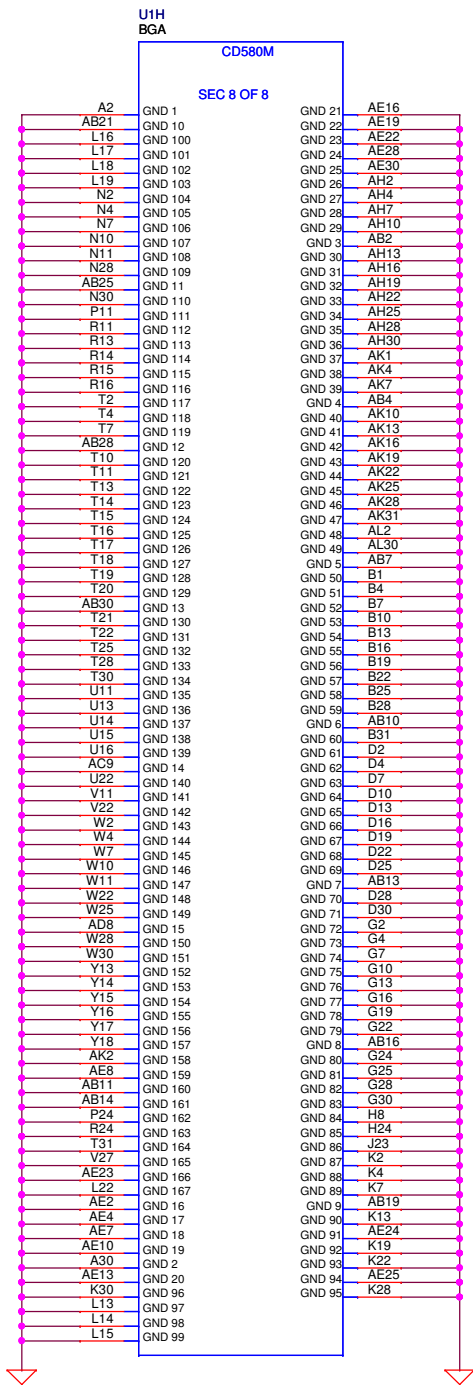




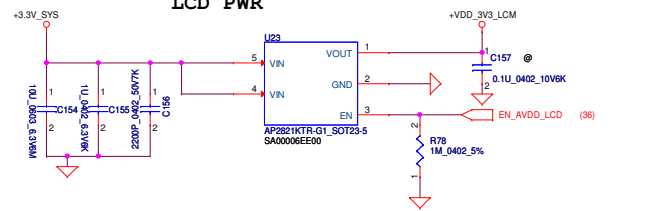
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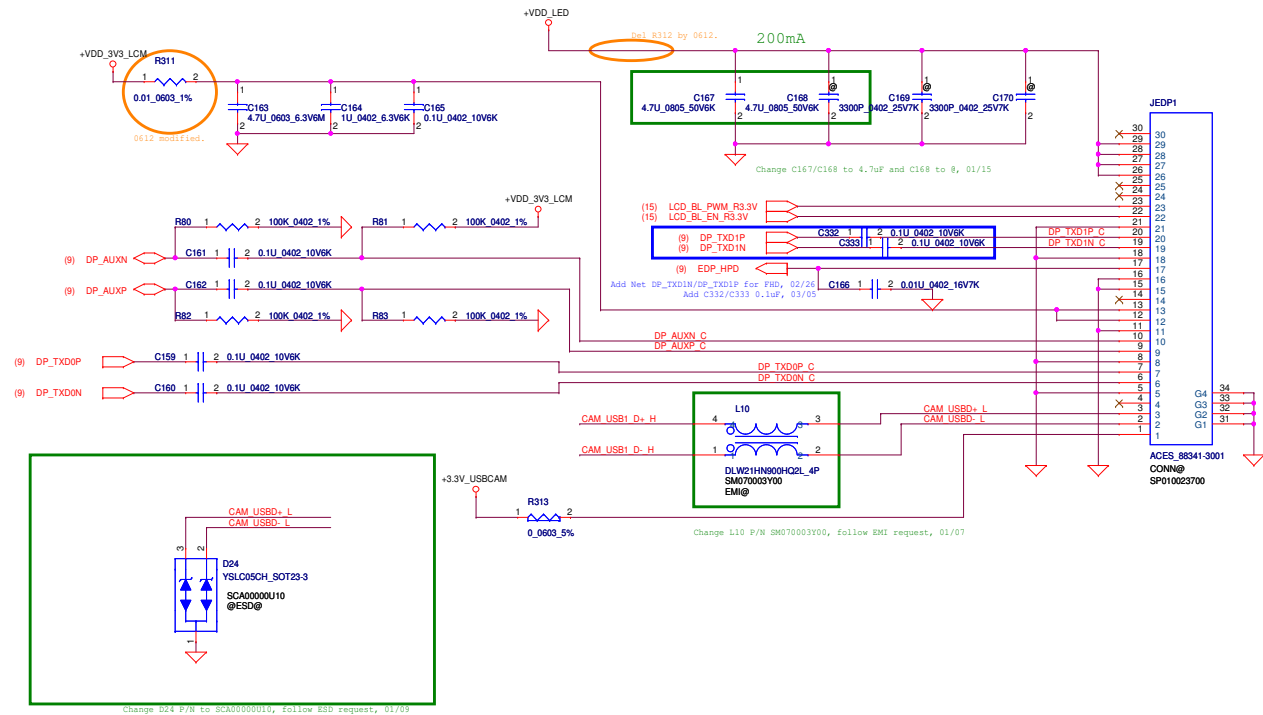
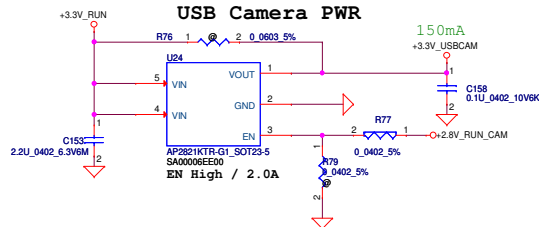
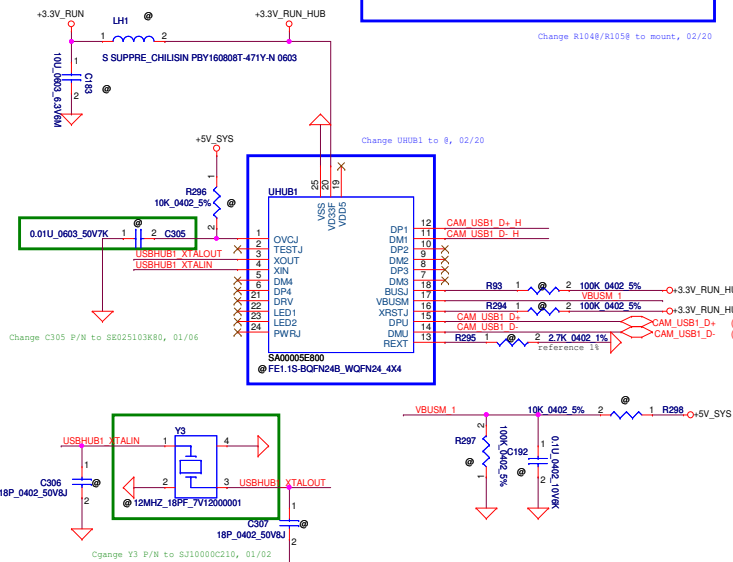
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Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title	POWER RAILS
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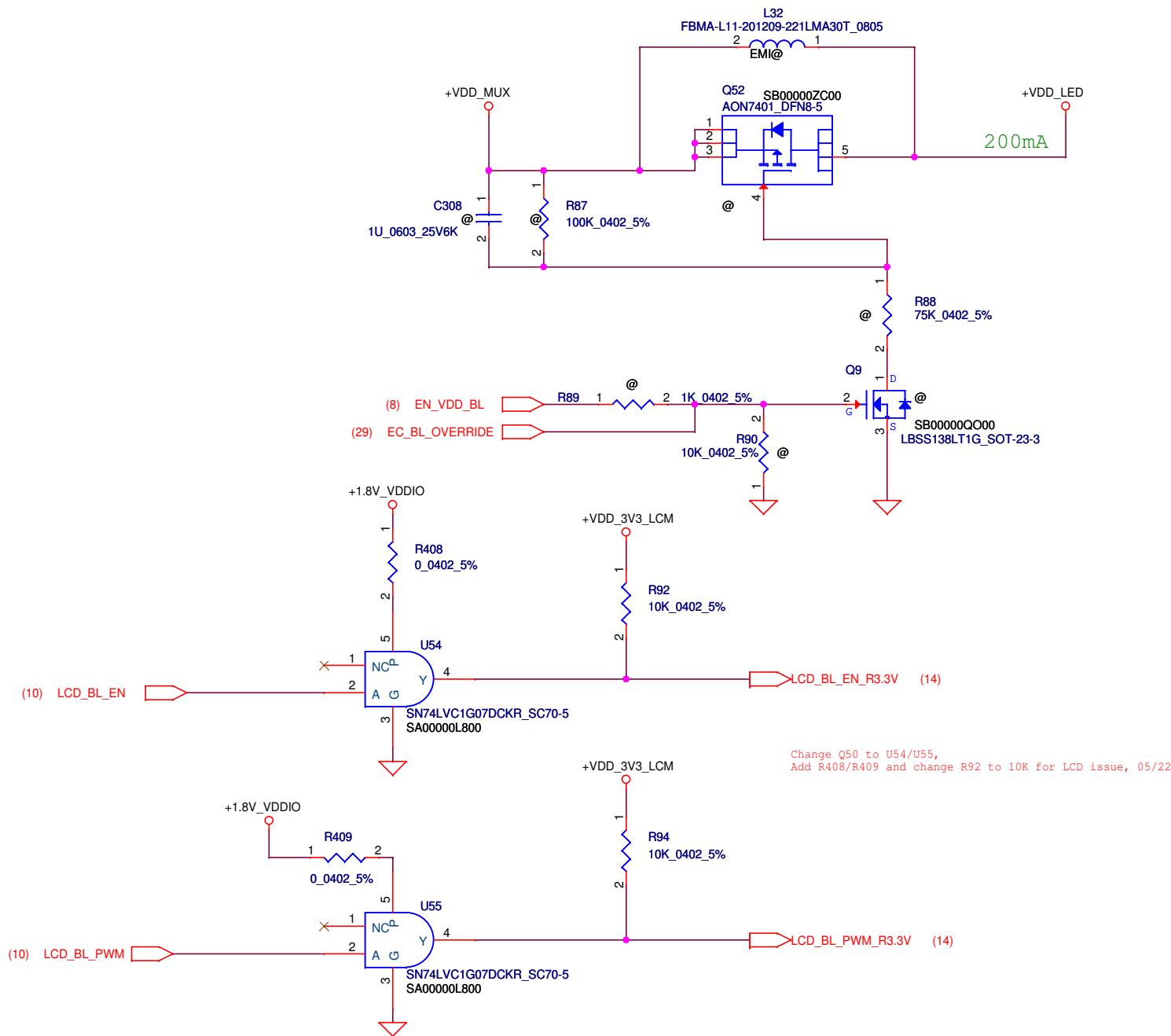
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title	CPU_GND	
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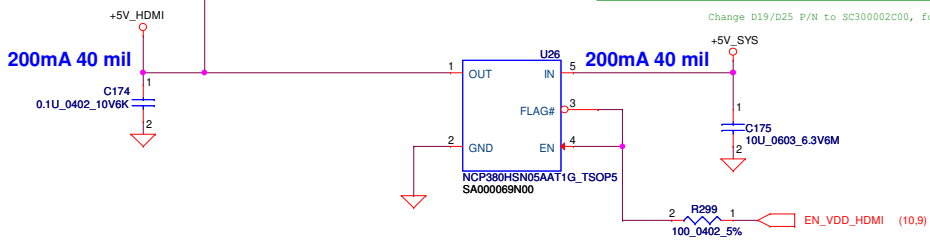
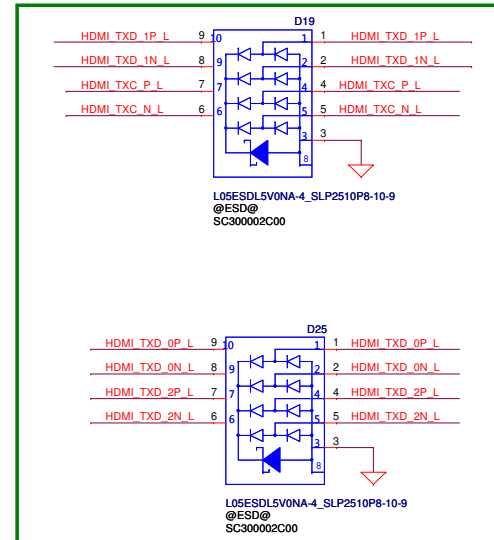
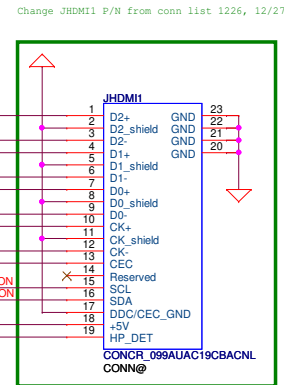
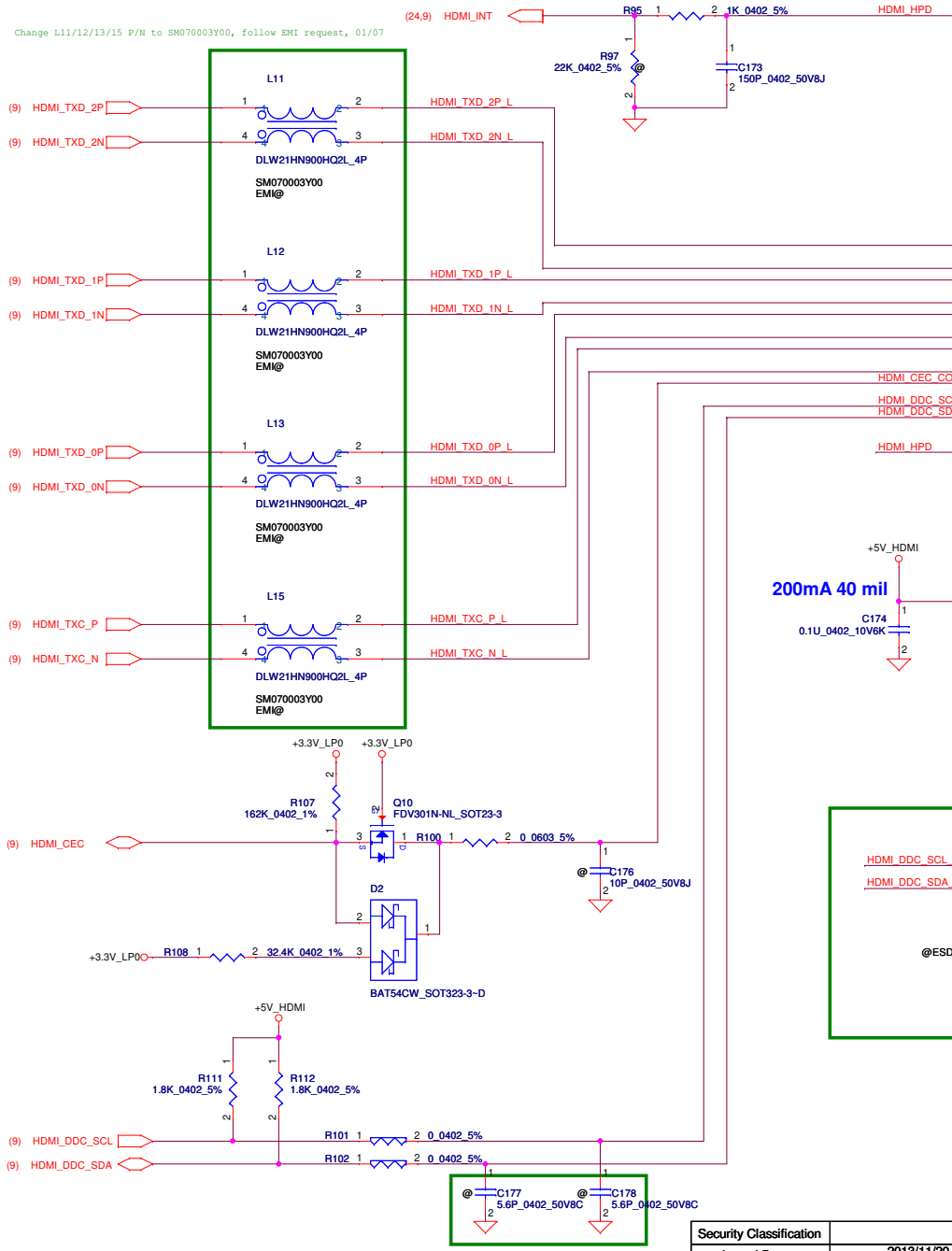
Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	TBD	0.8	[Watt]	Note 1/2
IDD	IDD Current	-	TBD	242	[mA]	Note 1/2
Irush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	



Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> EDP CONNECTOR	
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Date:	Thursday, June 19, 2014	ISheet	14	of	42



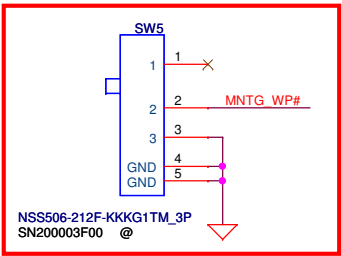
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title LCD BACKLIGHT	
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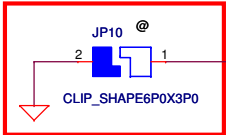
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title	HDMI TYPE D	
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WP Function	JP10(On)	JP10(Off)
SW5(Lock/Pin3)	WP	WP
SW5(Unlock/Pin2)	WP	Non WP



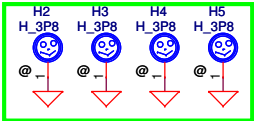
Add SW5 for write protect function, 04/14



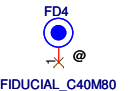
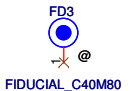
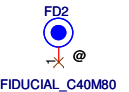
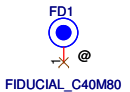
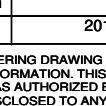
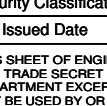
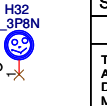
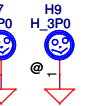
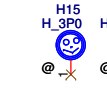
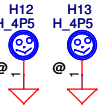
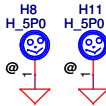
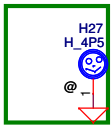
Change JP10 footprint to CLIP_SHAPE6P0X3P0, 04/09

(23) MNTG_WP#

CPU hold



Add H26/H27, 12/31
Delete H26, 01/03

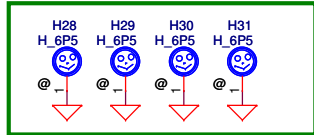


S1

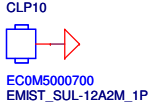
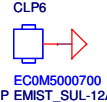
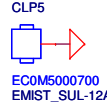


Frame @
EC176000800
Z3ENN_MB_RAM_FRAME_EMI

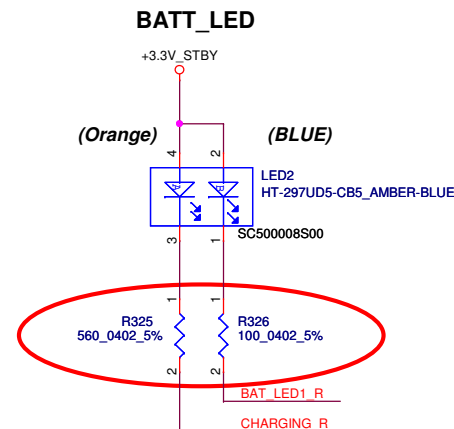
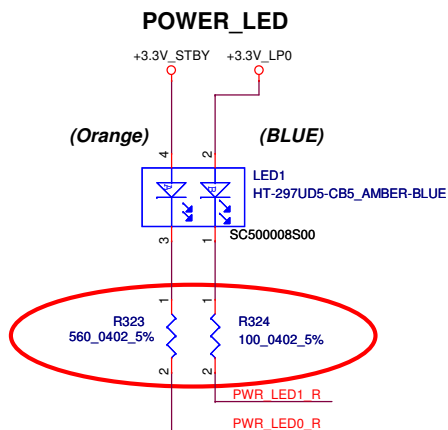
FUNCTION TABLE	
A Input	Y Output
L	L
H	Z



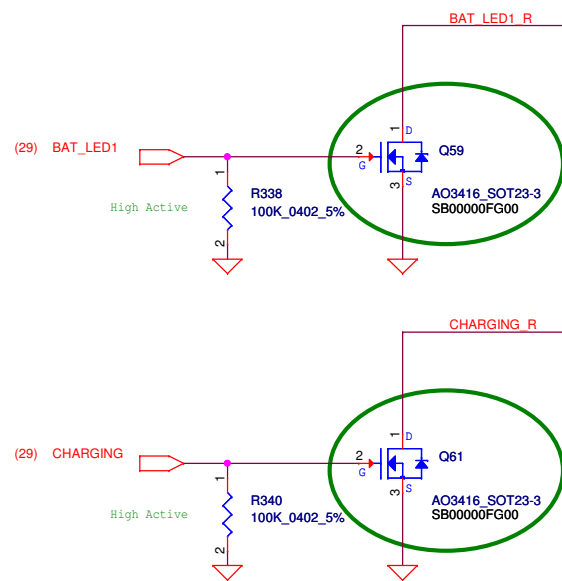
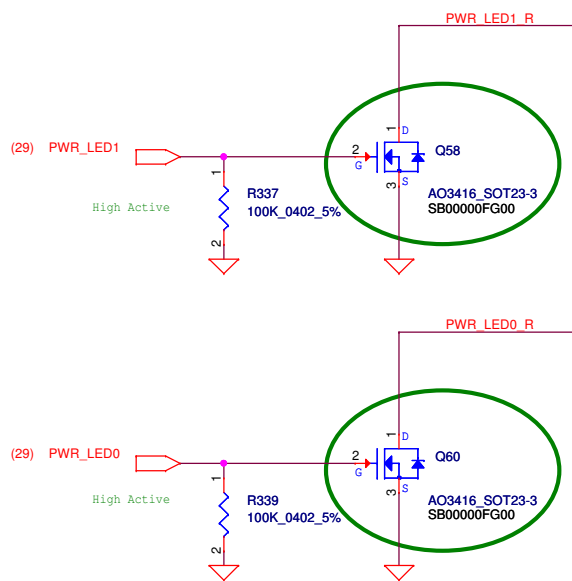
Add H28-H31 H_6P5, 01/13



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				Date	Thursday, June 19, 2014
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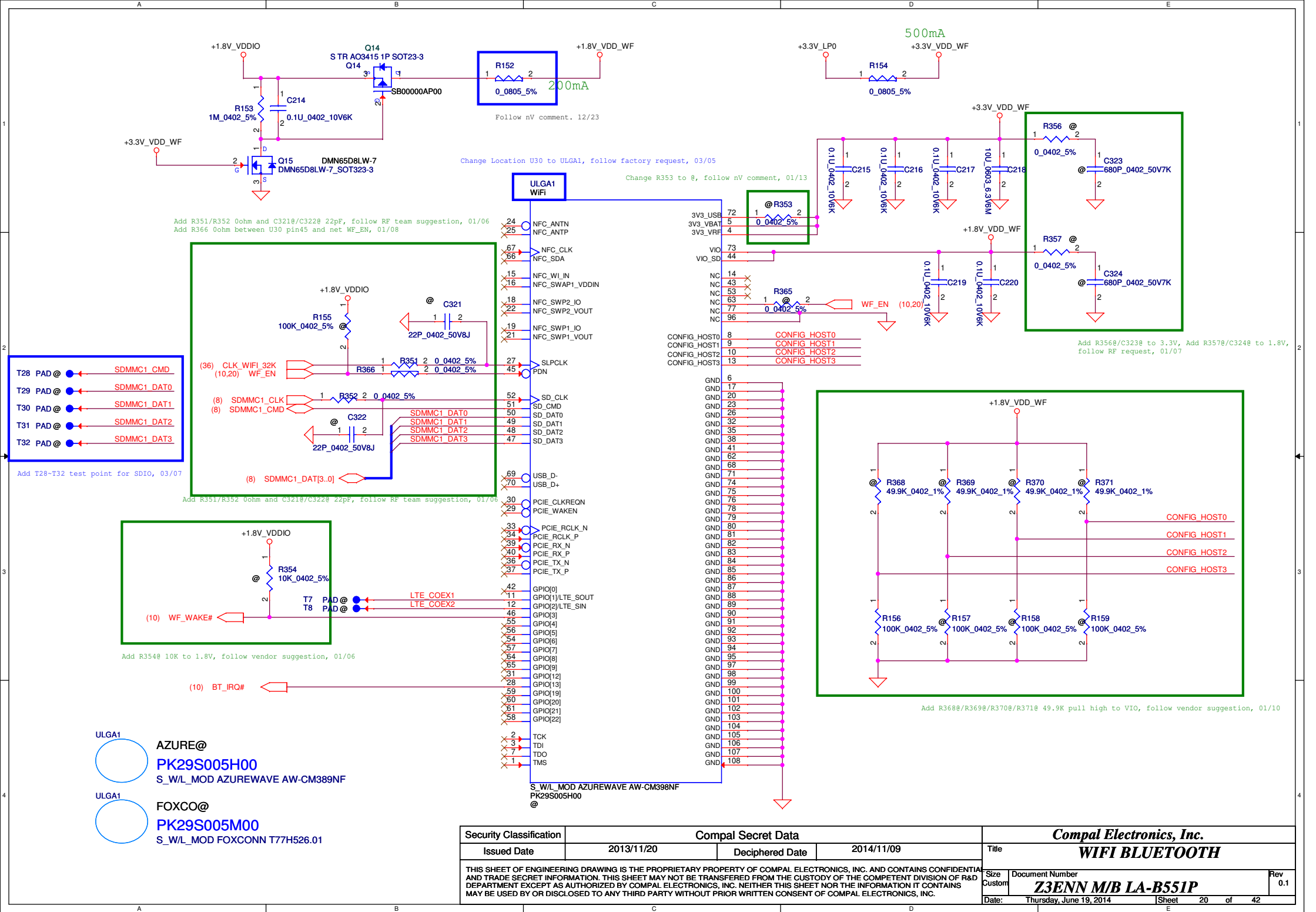


Change R324/R326 from 1K to 100 ohm,
Change R323/R325 from 2.2K to 560 ohm, 05/05

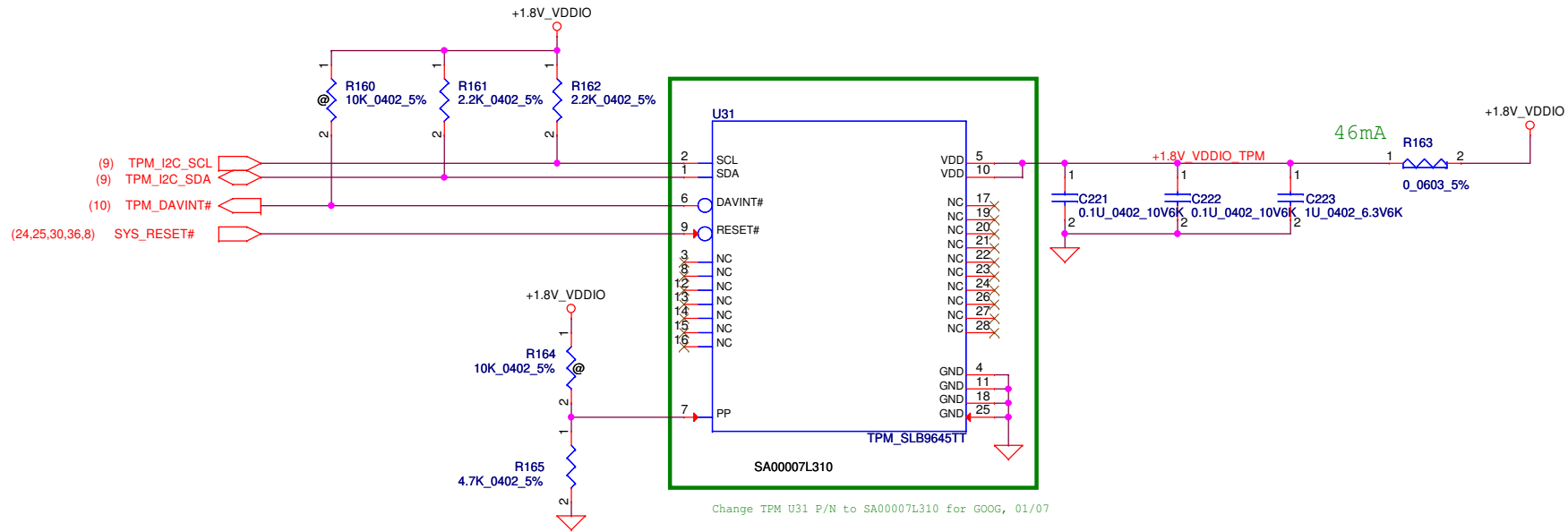


Change Q58-Q61 MOS to SB00000FG00, 01/15

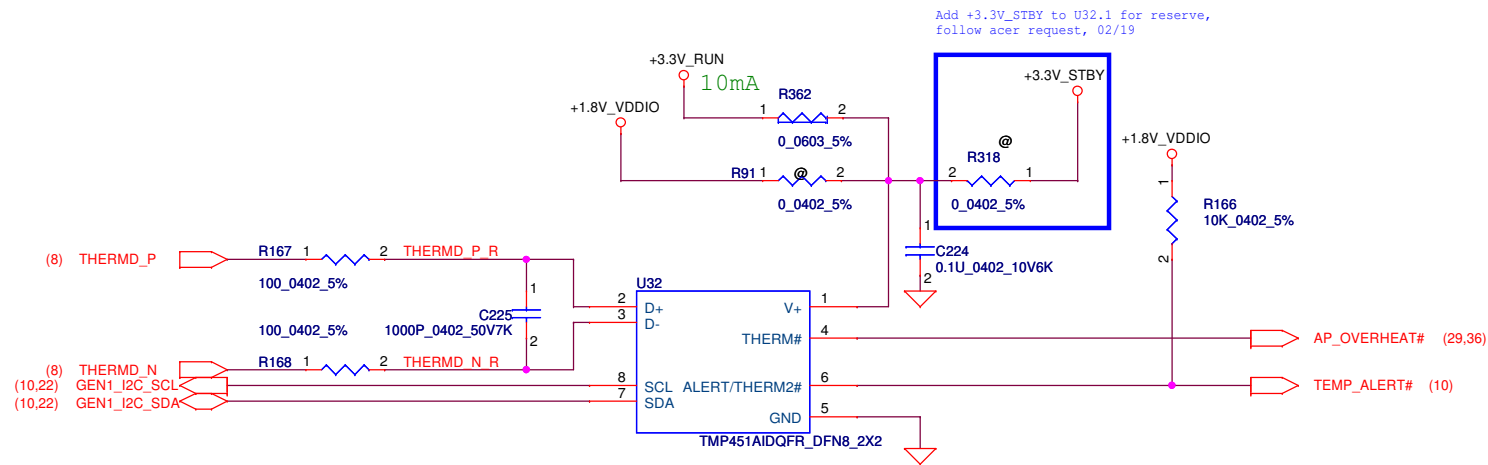
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title	LED
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Date: Thursday, June 19, 2014		Sheet 19 of 42		Document Number	Rev 0.1
				Z3ENN M/B LA-B551P	



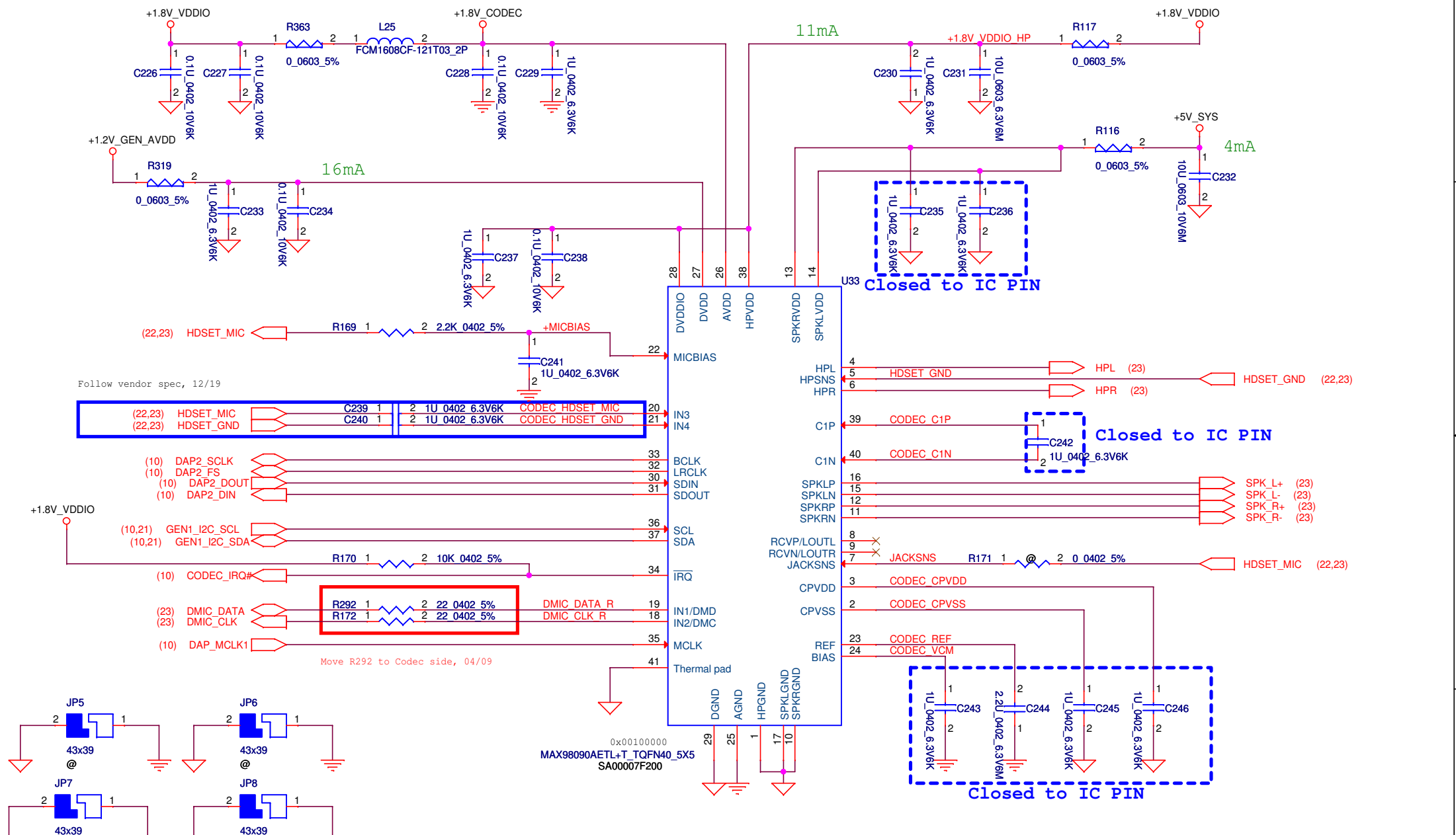
TPM



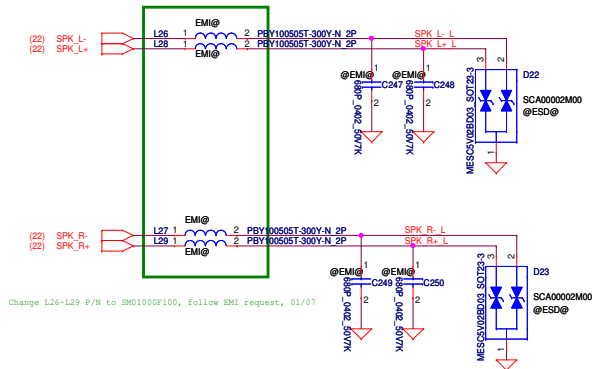
TEMP SENSOR



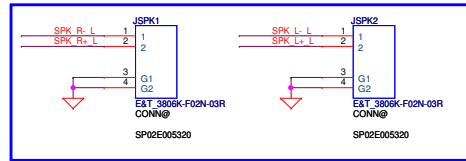
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title		
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				Custom	Z3ENN M/B LA-B551P	0.1
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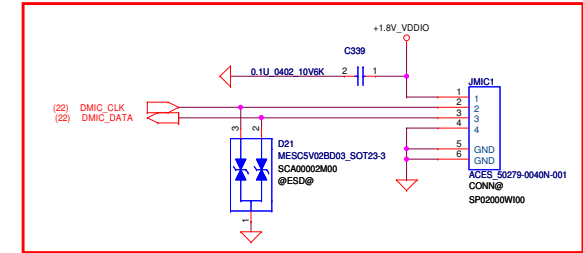
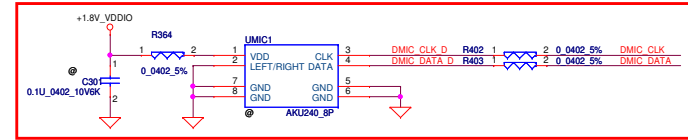
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/11/20	Deciphered Date	2014/11/09	Title AUDIO CODEC		
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Speaker Connector

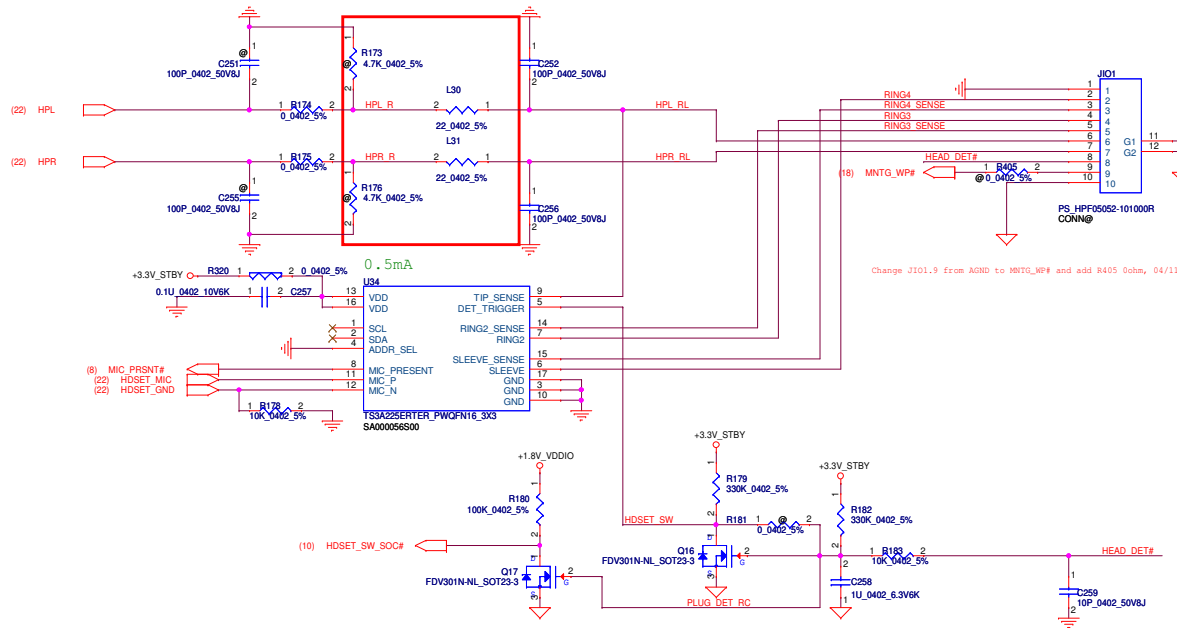


Digital MIC



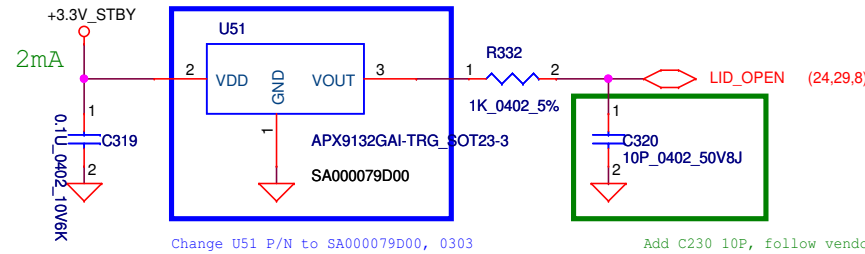
Change L30/L31 to 22ohm and R173/R176 to @ (un-mount) for audio issue, 05/12

Conn to Audio/B

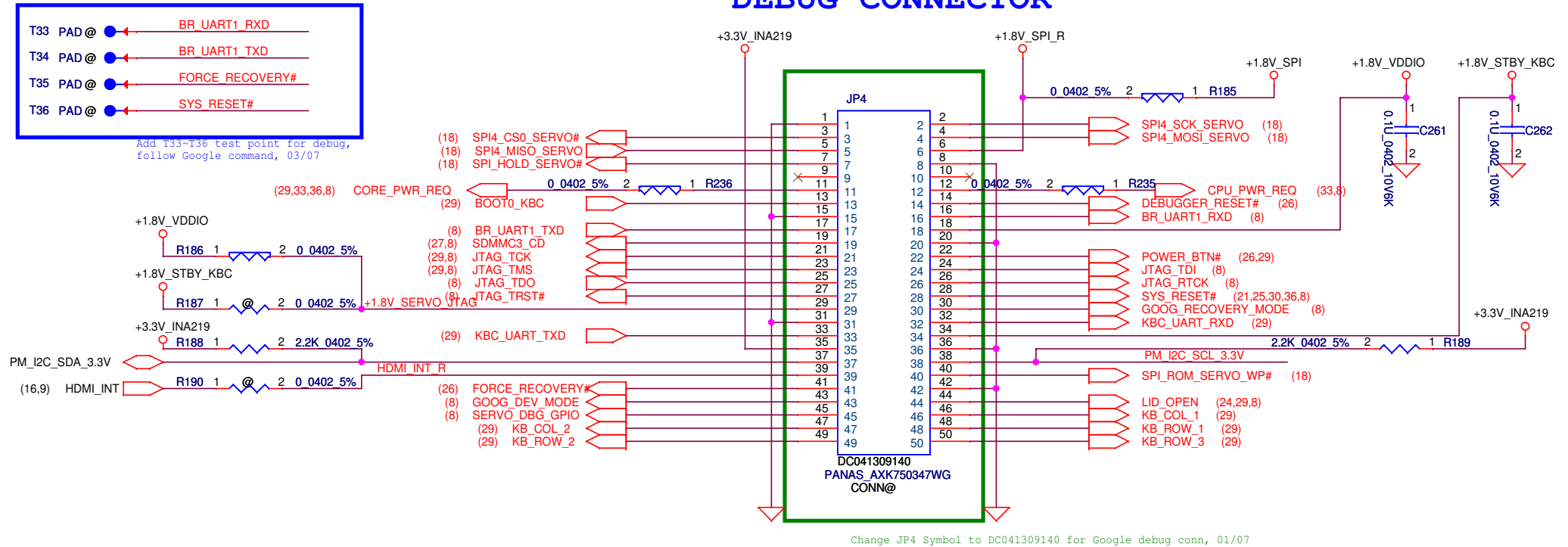


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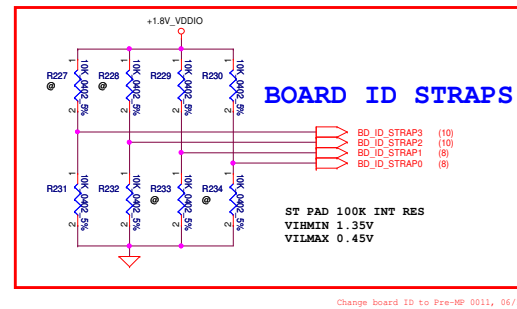
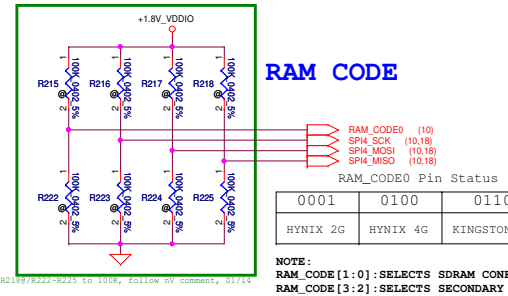
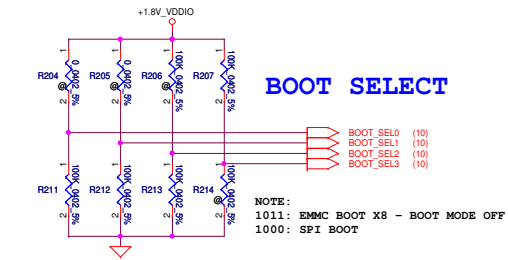
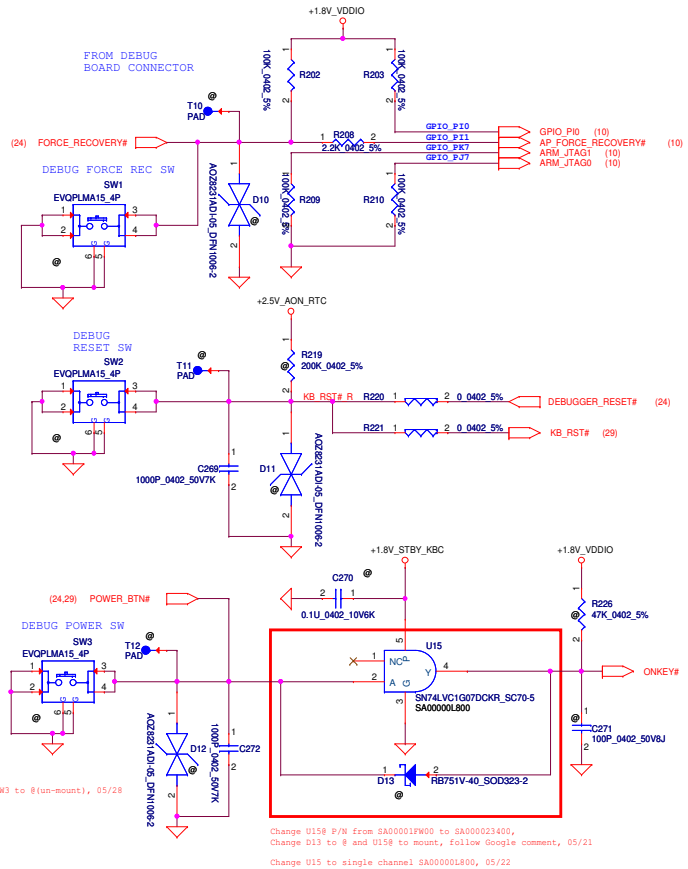
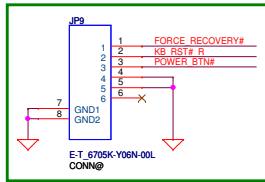
LID Sensor



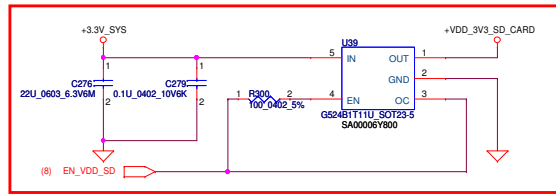
DEBUG CONNECTOR



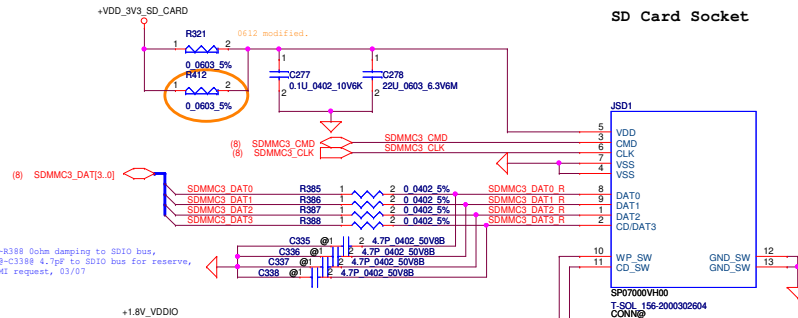
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Issued Date		2013/11/20		Deciphered Date		2014/11/09		Title DEBUG CONN/LID SENSOR							
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- R224 HYN2G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R223 HYN2G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R215 HYN2G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R217 HYN4G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R223 HYN4G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R222 HYN4G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R217 KIN2G@
SD028100380
S RES 1/16W 100K +-5% 0402
- R216 KIN2G@
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S RES 1/16W 100K +-5% 0402
- R222 KIN2G@
SD028100380
S RES 1/16W 100K +-5% 0402



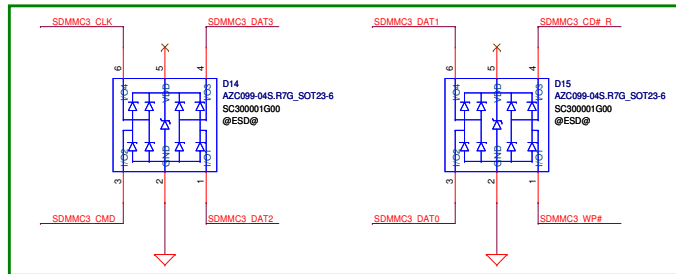
Change U39 from SA00007M800 to SA00006Y800, 0505



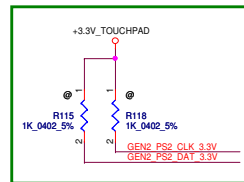
Add R385-R388 8ohm damping to SDIO bus,
Add C335-C338 4.7pF to SDIO bus for reserve,
Follow EMI request, 03/07

	PROTECT CONTACT	WRITE PROTECT POSITION	DETECT CONTACT
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN

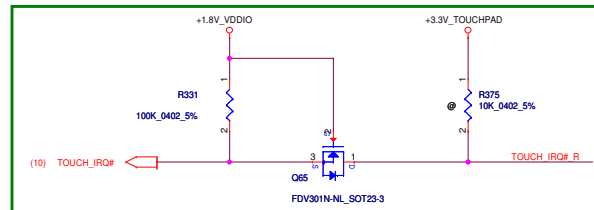
CLOSE : connect to GND
OPEN : Floating



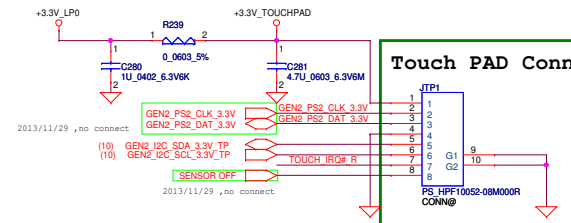
Change D14/D15 P/N to SC300001G00, follow ESD request, 01/07



Change R115/R118 to @ (un-mount), 01/14

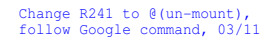


Add Q65/R375@ for TP 3.3V transfer to CPU 1.8V, 01/14



Change JTP1 P/N to SP01001A800, 01/02

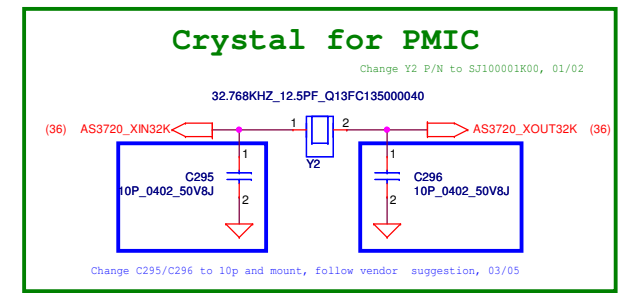
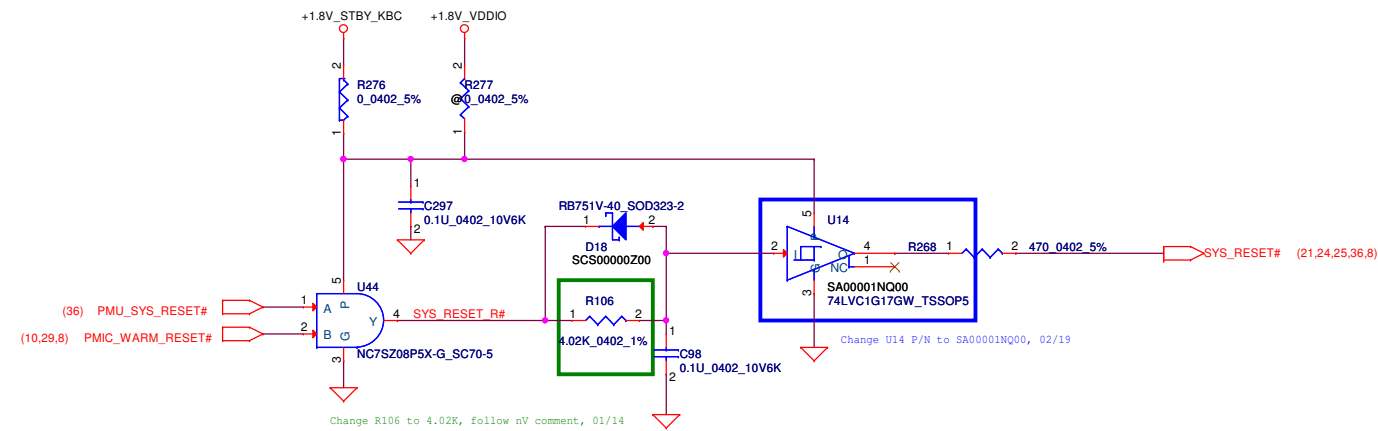
Add Q66/R376@ for TS 3.3V transfer to 1.8V, 01/15



Change R242 from 10K to 100K, if use U53 the pull high resistor have to mount, 04/11
Change Q66 to @ (un-mount),
U53 buffer and R242 100K pull high resistor change to mount, follow Google comment, 05/05

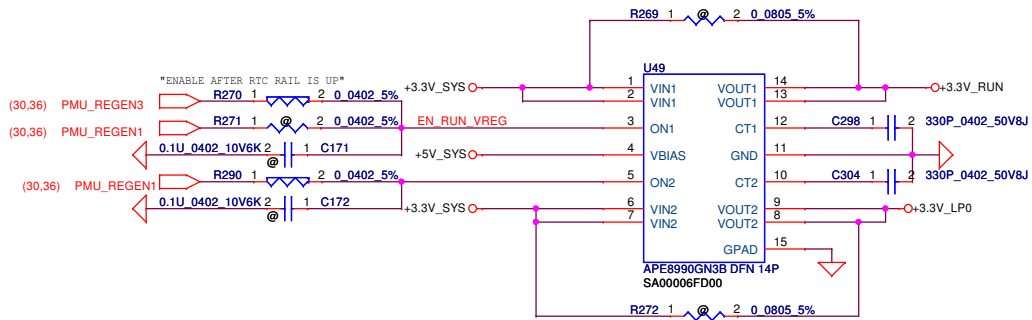
Add D29, follow ESD request, 01/07

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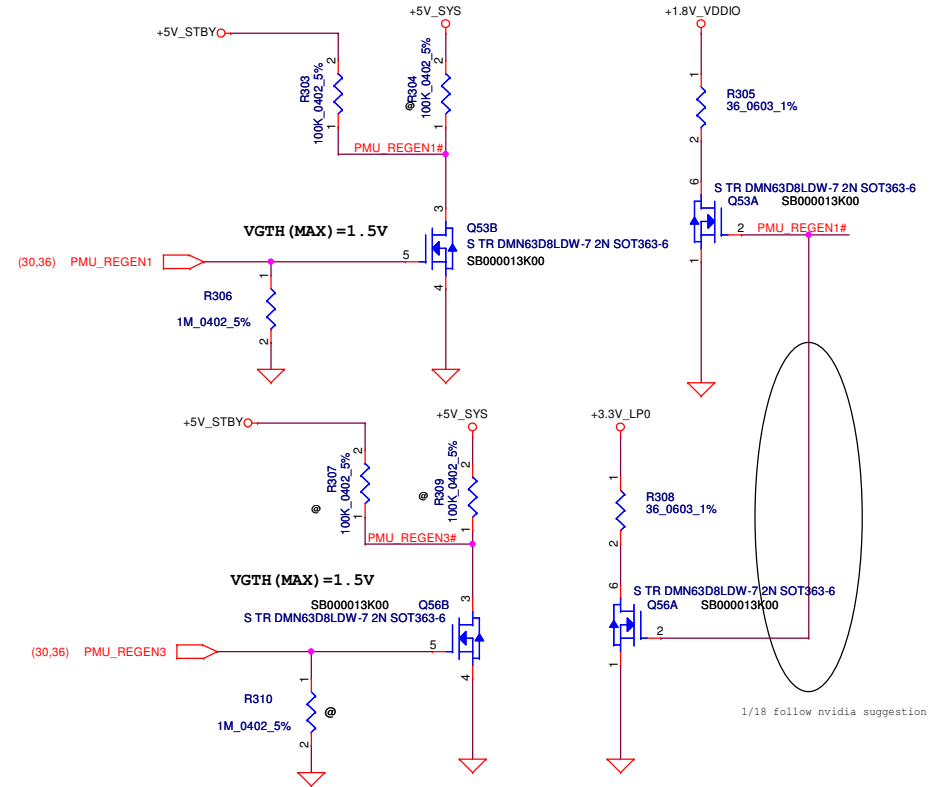
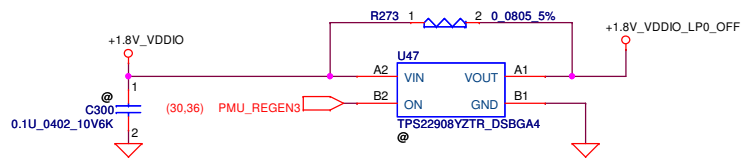


TEGRA +3.3V SEQUENCING
ENABLE AFTER RTC RAIL IS UP FOR RAILS OFF IN LP0

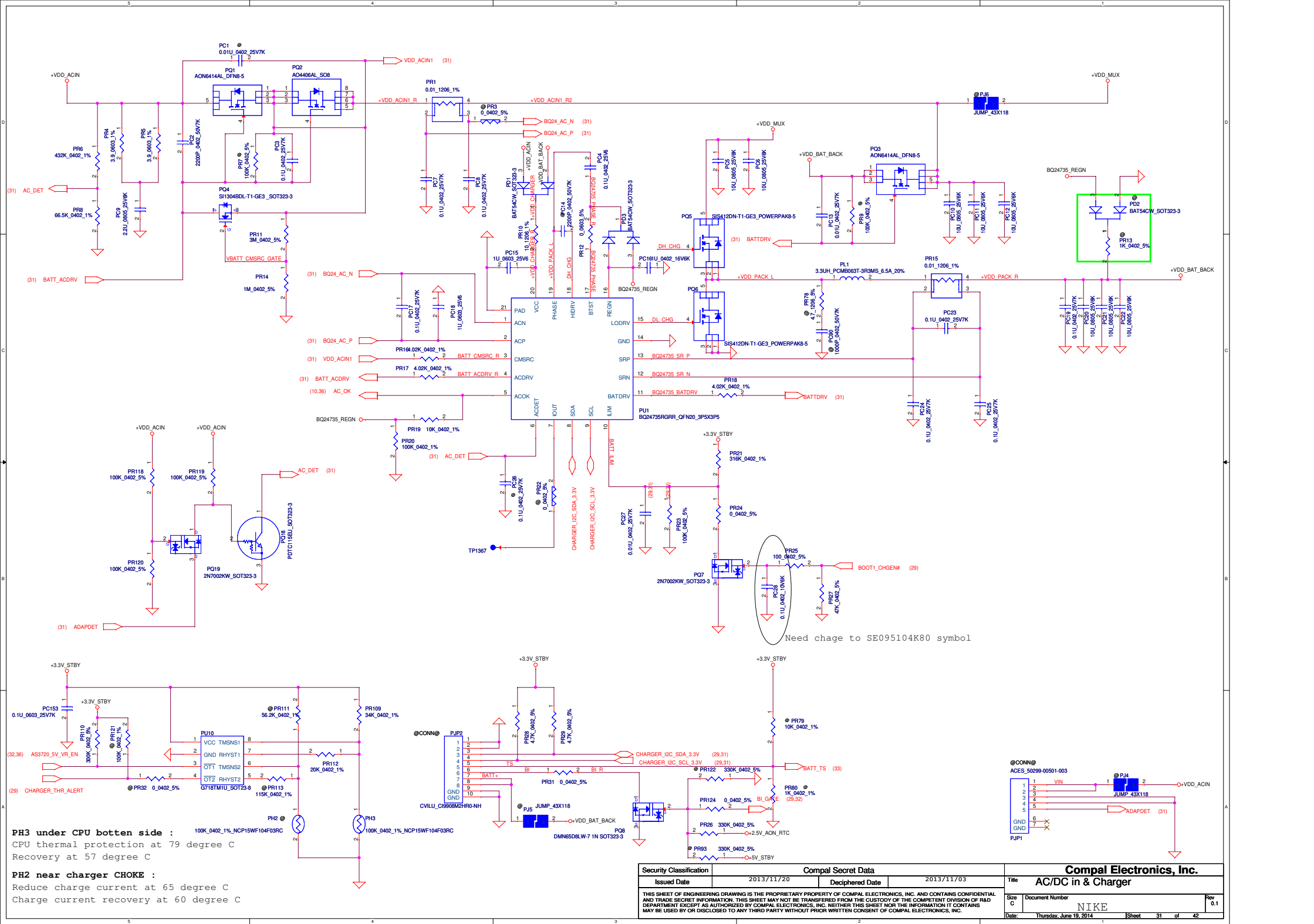
+3.3V VDD GATING FOR RAILS ON IN LP0



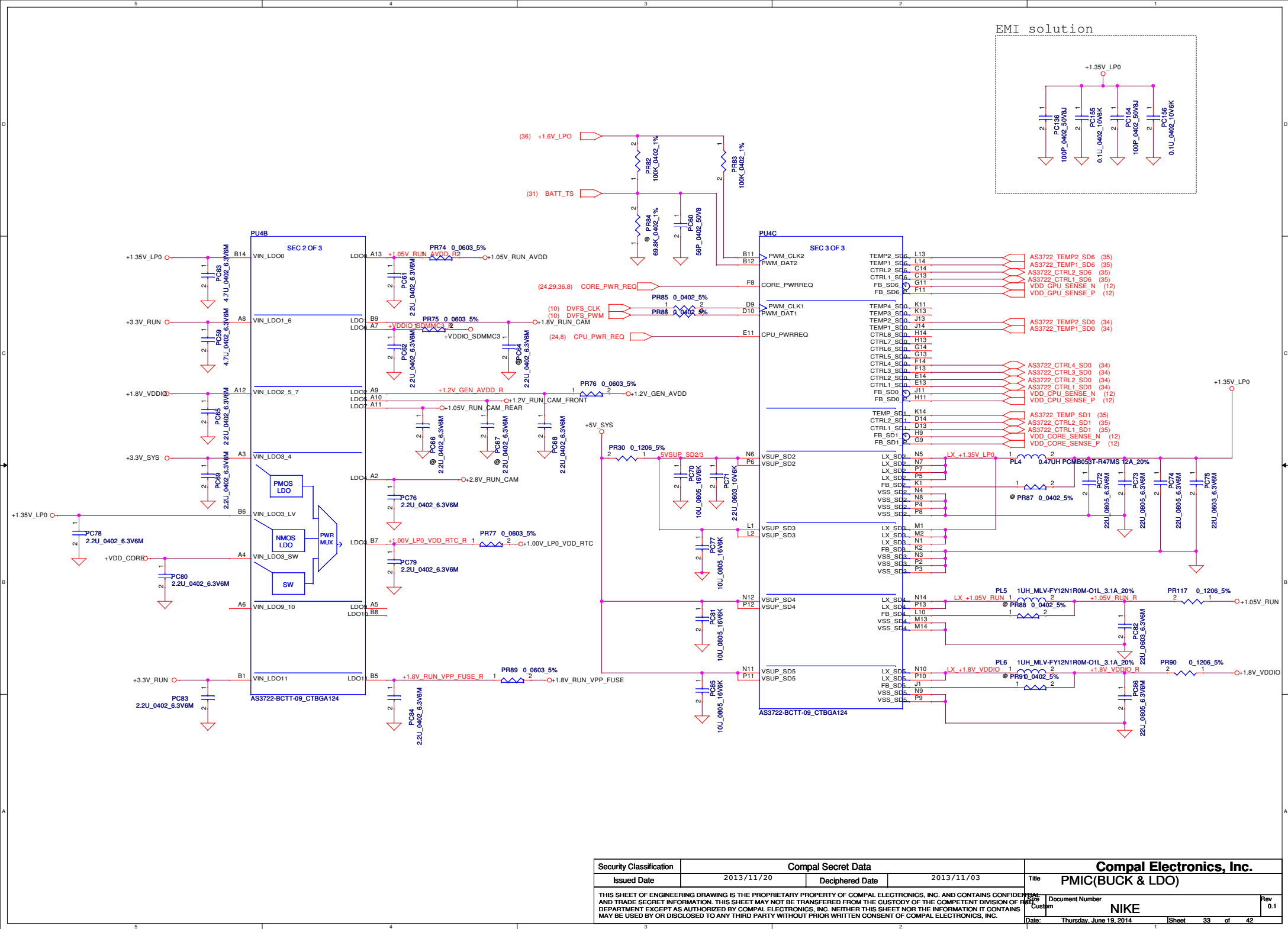
+1.8V VDDIO GATING
TEGRA +1.8V VDDIO SEQUENCING FOR RAILS OFF IN LP0



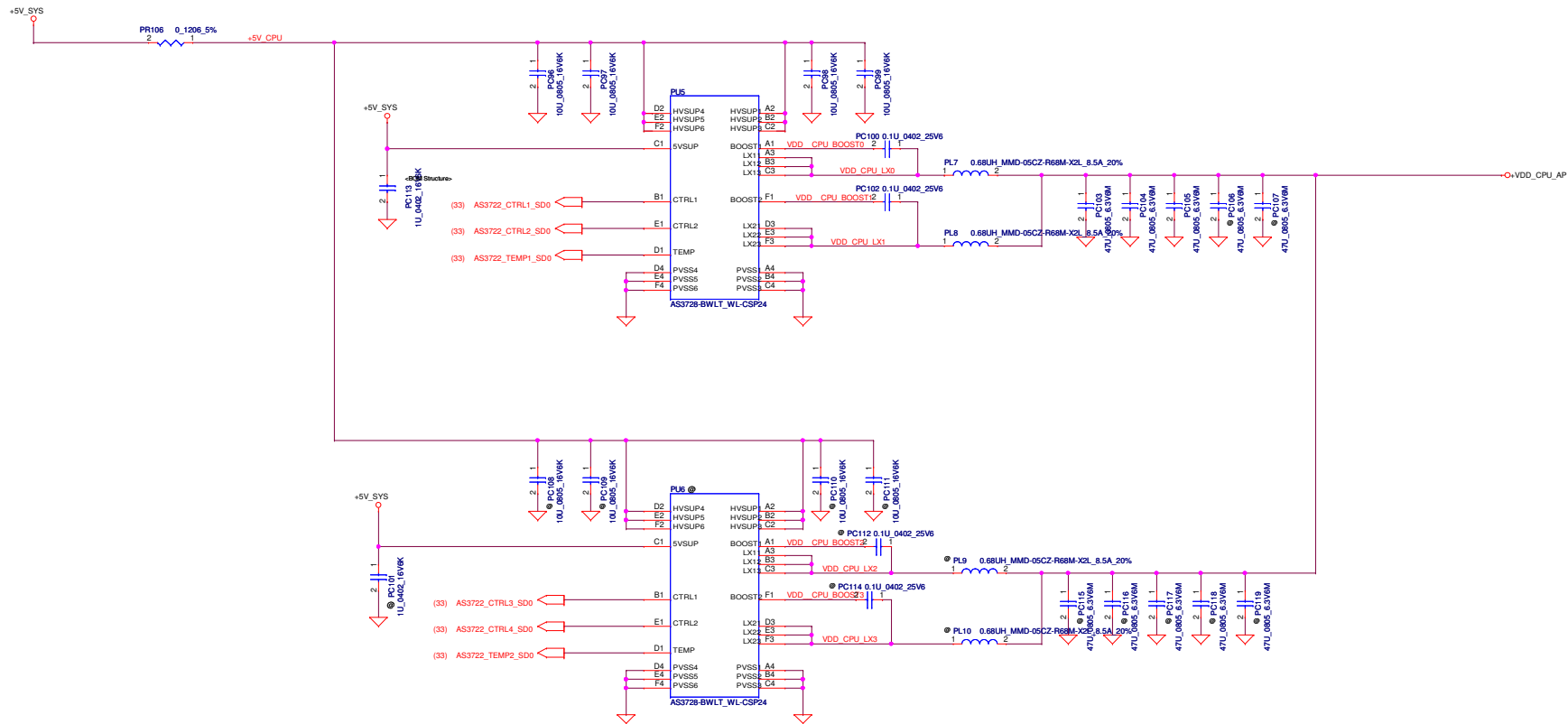
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2013/11/20		2014/11/09		Title	
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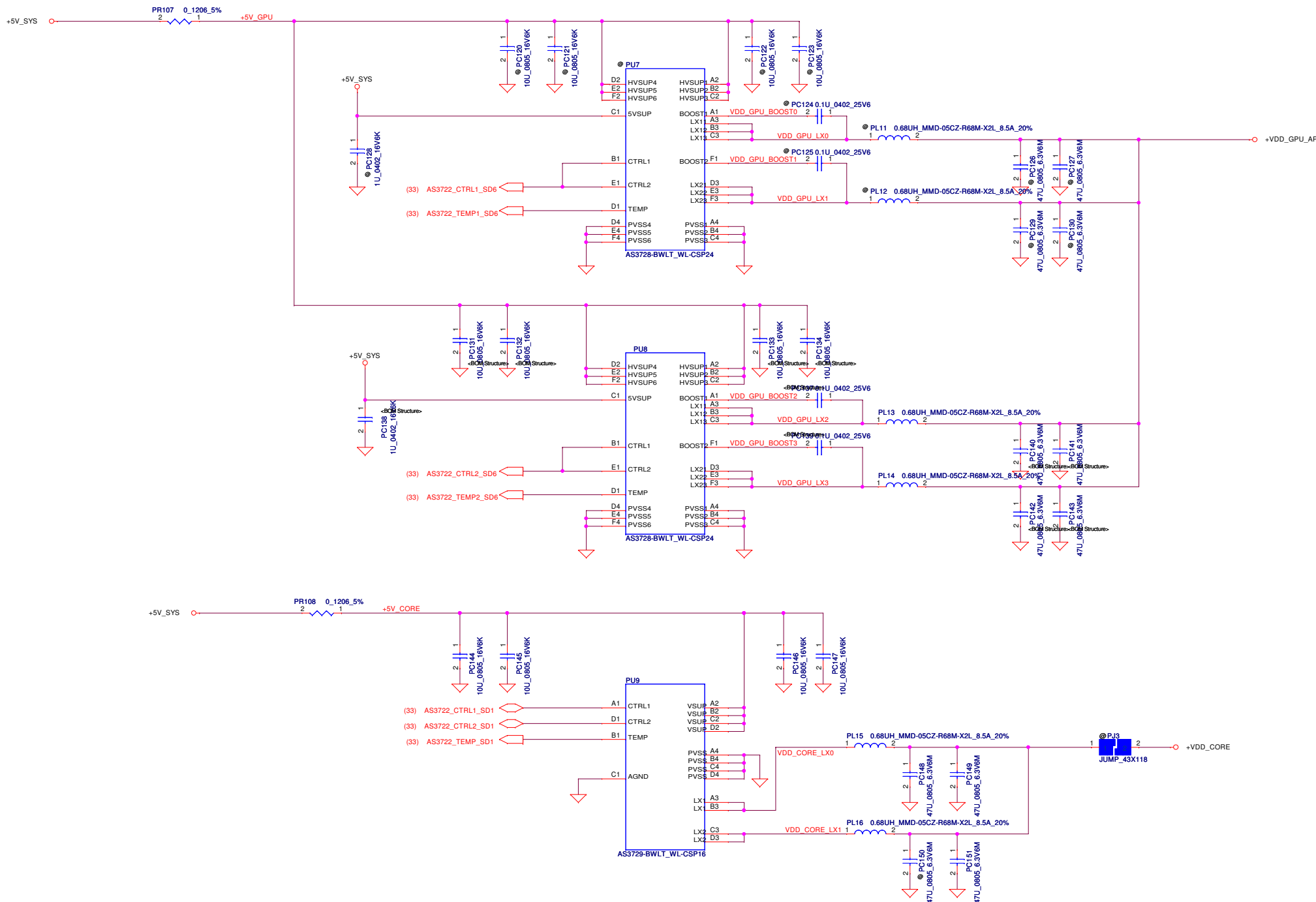


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